Curriculum Vitae, Dr. Jing Chen

Contacts

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Legal Status

- Canadian Permanent Resident
- Citizen of the People's Republic of China

Education

- 2014/09∼2020/06, Ph.D. CS, McGill University, Montreal, QC, Canada
  Supervisor: Dr. Xue (Steve) Liu
- 2010/09∼2012/07, M.Sc. CS, McMaster University, Hamilton, ON, Canada
  Supervisor: Dr. Christopher Anand
- 2005∼2009 M.Eng, Capital Normal University, Beijing, China

Areas of Interest

- Approximate Computing
- FPGA-based Hardware Accelerations
- High-level Synthesis (HLS)
- RISC-V, Application Specific Processor Designs
- Computer Architecture
- Digital Circuit Design

Publications

- **Jing Chen**, Jason H. Anderson: High-Level Synthesis of a Lightweight FPGA-Based RISC-V Processor, manuscript in submission.
- **Jing Chen**, Xue Liu, Jason H. Anderson: Software-Specified FPGA Accelerators for Elementary Functions, IEEE International Conference on Field-Programmable Technology (FPT 2018), **full paper accepted**. `https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8742300`

  Abstract: We use a high-level synthesis (HLS) methodology for the design of hardware accelerators for two elementary functions: reciprocal and square root. The functions are described in C-language software and synthesized into Verilog RTL using the LegUp HLS tool from the University of Toronto [1]. The accelerators are designed to deliver high accuracy, and provide less than 1 ULP error in comparison with GNU software (math.h). Through changes to the HLS constraints, hardware implementations with different speed/area trade-offs can be generated rapidly. In an experimental study, our HLS-generated accelerators are targeted to the Altera/Intel Cyclone V FPGA and compared with hand-designed cores from the FPGA vendor. Results show that our cores offer considerably better resource usage (area) (i.e. ALMs, DSPs, memory bits), while commercial cores operate at a modestly higher FMax.

- **Jing Chen**, Xue Liu: A High-Performance Deeply Pipelined Architecture for Elementary Transcendental Function Evaluation, IEEE International Conference on Computer Design (ICCD 2017), **full paper accepted**. `https://ieeexplore.ieee.org/document/8119212`

  Abstract: Many scientific applications rely on the evaluation of elementary transcendental functions (e.g. sin, cos, exp, log). Software math libraries are a popular approach for realizing such functions, and frequently use series expansion or lookup-table-based techniques. However, software approaches necessarily suffer from the traditional overheads of fetching/decoding instructions, limited cache sizes, and so on. In this paper, we present a hardware accelerator for such elementary transcendental functions that delivers high computational throughput. The accelerator design is generic in the sense that it is not tied to a specific function. However, we demonstrate its utility by accelerating logarithm. The proposed accelerator is applicable to a wide range of high-throughput scientific computing applications.

- **Jing Chen**, Xue Liu: A Fast and Accurate Logarithm Accelerator for Scientific Applications, IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP 2017), **poster paper accepted**. `https://ieeexplore.ieee.org/document/7995283`

Ongoing project

Apply high-level synthesis (HLS) technology to design RISC-V soft processor based on FPGA,

- My current project focuses on implementing 32-bit RISC-V integer instruction sets (RV32I) into multi-cycle soft processor for FPGA.
- The hardware implementation is specified in C software and synthesized by using LegUp HLS tool from University of Toronto.
- Our objective is to integrate basic single-precision floating-point arithmetic units (i.e. add, sub, mul, div) in conjunction with our elementary function hardware accelerators (i.e. log, recip, sqrt) into the RISC-V soft processor to better accommodate computation intensive applications.

Theses

Doctor, McGill University — Montreal, Quebec, Canada

- Thesis Title: Hardware Acceleration for Elementary Functions and RISC-V Processor
- I mainly have accomplished three research packages:
  - Design and implementation of floating-point reciprocal accelerators.
  - Design and implementation of floating-point square root accelerators.
  - Design and implementation of a RISC-V soft processor.

Master, McMaster University — Hamilton, Ontario, Canada

- Thesis Title: A Pipelined, Single Precision Floating-point Logarithm Computation Unit (LCU) in Hardware.
- It developed a method to implement mathematical function in hardware (circuit level) computation unit.
- LCU was lookup table based and used non-linear interpolation.
- LCU was implemented by VHDL, schematics under Altera Quartus II design software.
- We have estimated LCU was able to evaluate 2.9G single precision values per second (in ASIC) and maintained at least 21-bit accuracy (full accuracy is 23-bit).

- To the best of my knowledge, the throughput of the state-of-art logarithm approximation unit was 353.5MHz, while it maintained 14-bit accuracy (in 2012).
- My thesis was funded by the IBM Center for Advanced Studies and was available on `https://macsphere.mcmaster.ca/bitstream/11375/12364/1/fulltext.pdf`

Undergraduate, Capital Normal University Beijing, China

- My thesis presented a 16-bit RISC-like system model. It contained two parts, both were started from scratch:

  A RISC-like instruction set (46 instructions).

  A 16-bit multi-cycle processor (2000 lines of VHDL, Schematic, FPGA).

Talk

Presenter, McGill CS System Seminar May 2018

- Delivered a presentation about my new paper under submission titled "High-Level Synthesis of FPGA Hardware Accelerators for Elementary Functions" to professors and graduate students in CS department.
- Answered questions and received feedbacks.

Presenter, McGill CS System Seminar Oct 2017

- Delivered a presentation about my ICCD paper titled "A High-Performance Deeply Pipelined Architecture for Elementary Transcendental Function Evaluation" to professors and graduate students in CS department.
- Answered questions and received feedbacks.

Presenter, IBM Markham Research Center Summer 2012

- Delivered a presentation about my master's thesis to the IBM FPGA team.
- Answered questions and discussed the potential improvements.

Work Experience

Teaching Assistant, McMaster University Winter 2012

- Teaching assistant in a third year"Databases"course.
- Delivered 1 tutorial/week to 40 students.
- Answered questions on an individual basis where needed.
- Invigilate two midterm exams.
- Graded individual assignments and tests.

Teaching Assistant, McMaster University Winter 2011

- Teaching assistant in a third year"Machine-level Programming"course.
- Graded individual assignments and tests.

Teaching Assistant, Capital Normal University Winter 2009

- Teaching assistant in a third year"Computer Architecture and CPU Design"course.
- Wrote teaching materials.
- Answered questions in VHDL programming on an individual basis.
- Assisted students to learn how to handle EDA tools and FPGA boards.

Honors

- McGill Graduate Excellence Scholarship, 2019
- Croucher Foundation sponsorship of Summer Course on Performance-Aware Programming using Application Accelerators, May, 2018
- McGill Graduate Award Recipient, Feb, 2018
- McGill CS Great Travel Grant Recipient, Oct, 2017
- ASAP'17 Student Travel Grant Recipient, May, 2017
- McGill Graduate Excellence Scholarship, 2014 to 2015
- IBM Centre for Advanced Study (CAS) Research Project Fellowship, 2011
- McMaster Graduate Student Entrance Award, 2010
- Capital Normal University 3rd Grade Scholarships, 2006, 2007, 2008
- Capital Normal University Excellent Intern, 2008
- Capital Normal University Second Prize of Undergraduate Research Project, 2008

Academic Activity

- Attended 2019 Neural-Network Optimised VLSI Accelerators (NOVA) Summer Course (NOVA'19, Zhuhai, China)
- Attended 2018 IEEE International Conference on Field-Programmable Technology (FPT'18, Naha, Okinawa, Japan)
- Attended 2018 Croucher Summer Course on Performance-Aware Programming using Application Accelerators (PAPAA'18, HongKong, China)
- Attended 2018 ACM International Symposium on Highly Efficient Accelerators and Reconfigurable Technologies (HEART'18, Toronto, Ontario, Canada)
- Attended 2018 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA'18, Monterey, California, United States)
- Attended 2017 IEEE International Conference on Computer Design (ICCD'17, Boston, Massachusetts, United States)
- Attended 2017 IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP'17, Seattle, Washington, United States)
- Attended 2016 IBM CASCON (Markham, Ontario, Canada)
- Attended 2015 IBM CASCON (Markham, Ontario, Canada)

Service

- Served as TA for Neural-Network Optimised VLSI Accelerators (NOVA) Summer Course (2019)
- Reviewed one article from Transactions on Mathematical Software (TOMS, Oct, 2018)
- Reviewed one article from Transactions on Reconfigurable Technology and Systems (TRETS, Oct, 2017)
- Reviewed one article from IEEE Communications Surveys and Tutorials (COMST, June, 2016)
- Reviewed one article from IEEE Transaction on Services Computing (Jan, 2016)
- Reviewed four articles from IEEE International Conference on Computer Communications (INFOCOM, Sep, 2015)
- Reviewed one article from IEEE International Conference on Distributed Computing Systems (ICDCS, Oct, 2014)
- Served as volunteer for McMaster outreach program called Grade 8 Girls (2014)

Computer Skills

Programming Languages: C, VHDL, Matlab, LATEX, HTML
Software Development IDEs: IntelliJ, Eclipse, Netbeans
Hardware Simulators: LegUp HLS, Altera Quartus II, ModelSim, DE2-70
Databases: SQL, Relational Algebra, IBM DB2
OS: Windows, Ubuntu, iOS