On Bus Graph Realizability*

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Abstract

We consider the following graph embedding problem: Given a bipartite graph $G = (V_1, V_2; E)$, where the maximum degree of vertices in V_2 is 4, can G be embedded on a two dimensional grid such that each vertex in V_1 is drawn as a line segment along a grid line, each vertex in V_2 is drawn as a point at a grid point, and each edge $e = (u, v)$ for some $u \in V_1$ and $v \in V_2$ is drawn as a line segment connecting u and v, perpendicular to the line segment for u? We show that this problem is NP-complete, as well as related problems.

1 Introduction

Orthogonal graph drawing is a well studied area in graph drawing. In this paper, we study orthogonal drawings of *bus graphs*, which represent interconnectivity of functional entities in a chip. In VLSI layouts, a *bus* is a line segment drawn on a plane. To establish a connection among a collection of buses, a *connector* is drawn as a point on the plane, and then joined to the buses by line segments. Thus, the interconnections of the buses can be represented by a bipartite graph, where one partition of vertices corresponds to the set of buses, and the other corresponds to the set of connectors. We call such bipartite graphs *bus graphs*, and ask whether they have certain grid drawings. Bus graph realizability (BGR) problem is defined as follows.

BGR Instance: A bipartite graph $G = (\mathcal{B}, \mathcal{C}; \mathcal{E})$ such that $\forall c \in \mathcal{C}$, $\deg(c) \leq 4$.

Question: Can G be drawn onto a grid so that the following properties hold?

1. Each vertex $B \in \mathcal{B}$ is drawn as a closed line segment along a grid line.
2. Each vertex $c \in \mathcal{C}$ is drawn at a grid point.
3. Each edge $(B, c) \in \mathcal{E}$ is drawn as a closed line segment between B and c, that is perpendicular to B, and contains no other connectors or buses apart from B and c; an edge can, however, cross other edges as shown in Fig. 1.
4. No buses or connectors may intersect.

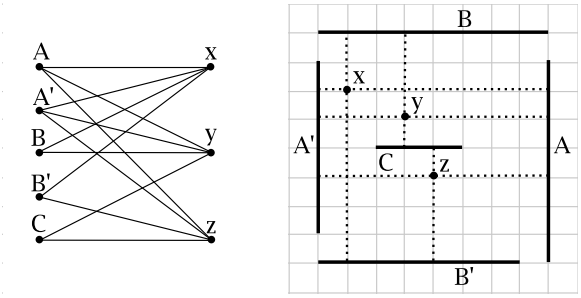

Figure 1: A bus graph and its realization. This graph is a gadget called an (A, B)-perp, defined in Sect. 3

We say a bus graph G is *realizable* if G can be drawn while meeting the conditions above. See Fig. 1. Now we are ready to state our main result.

Theorem 1 *BGR is NP-complete.*

Furthermore, Sect. 4 studies several related problems.

Related Work. The orthogonal graph drawing style has found many applications in VLSI design since its introduction in [8]. A realization of a bus graph conveys visibility relations among the buses and connectors. Given an arrangement of points (connectors) and axis-parallel line segments (buses) on a grid, if a bus B_i and a connector c_j can be joined by a straight-line edge, then there exists an axis-parallel line of sight that does not intersect any buses or connectors except B_i and c_j. Furthermore, if all the buses are drawn horizontally, the bus graph G is a subgraph of the visibility graph representing the vertical visibility among the bus segments. There is an abundance of prior work on the visibility graphs based on axis-parallel lines of sight. In particular, [9] and [7] study bar visibility graphs (BVGs), where each vertex in the graph is drawn as a horizontal line segment in R^2, and the adjacency among the vertices represent vertical visibility. The recognition problem of such graphs can be solved in linear time. In [1, 2, 4, 5, 6], the authors study rectangle visibility graphs (RVGs), where each vertex is drawn as a rectangle, and the adjacency among the vertices represent axis-parallel lines

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of sight. Reference [5] shows that the recognition problem of such graphs is NP-complete. The bus graphs studied here can be regarded as related to RVGs, where the vertices are restricted to degenerate rectangles such as line segments and points.

2 Preliminaries

Given a bus graph $G = (\mathcal{B}, \mathcal{C}; \mathcal{E})$, we call a vertex B a $\mathcal{B}$-vertex if $B \in \mathcal{B}$; its realization is called a *bus*. Similarly, a $\mathcal{C}$-vertex refers to a vertex in $\mathcal{C}$, and its realization is called a *connector*. Uppercase letters denote $\mathcal{B}$-vertices, and lowercase letters denote $\mathcal{C}$-vertices.

We use a function Γ to denote an embedding of a combinatorial bus graph G. For example, $\Gamma(c)$ for some $\mathcal{C}$-vertex c denotes the grid point where c is laid out, and $\Gamma((B, c))$ for some edge (B, c) denotes the line segment along a grid line where (B, c) is laid out.

Note that many variations of the bus graph problem can be devised, yet several are equivalent. For example, suppose the buses are realized as *open* line segments. It is not hard to see that this variation is equivalent to the problem stated in Sect. 1.

For another variation, note that a bus graph $G = (\mathcal{B}, \mathcal{C}; \mathcal{E})$ can be regarded as a hypergraph, where $\mathcal{B}$ is the set of vertices, and $\mathcal{C}$ is the set of hyperedges, each connecting at most four vertices. In this context, it is of interest to see if the realizability problem changes if we disallow multiple hyperedges in the hypergraph G. In other words, we would assume that no two $\mathcal{C}$-vertices are adjacent to the same set of $\mathcal{B}$-vertices. As the following lemma shows, this assumption does not change our problem.

Lemma 2 *Let G be a bus graph with multiple hyperedges in $\mathcal{C}$, and let G' be the bus graph constructed from G by removing hyperedge duplicates. Then G is realizable if and only if G' is realizable.*

3 NP-Completeness

We now show the hardness of BGR. First, it is easy to show that the problem is in NP: if a bus graph G is realizable, there exists a compact layout such that the size of the layout is linear in each dimension. To see this, we can take any layout of G, and then compact the layout so that the layout is bounded by a box of $O(n) \times O(n)$ size.

Lemma 3 *BGR is in NP.*

We prove the NP-hardness of BGR by a reduction from NAE-3SAT [3]. First we introduce and discuss properties of several gadgets.

Definition 4 *An (A, B)-perp is a bus graph component consisting of three $\mathcal{C}$-vertices, five $\mathcal{B}$-vertices, and twelve edges as shown in Fig. 1.*

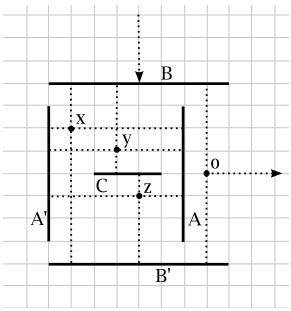

Figure 2: An embedding of a (B, o)-flipper.

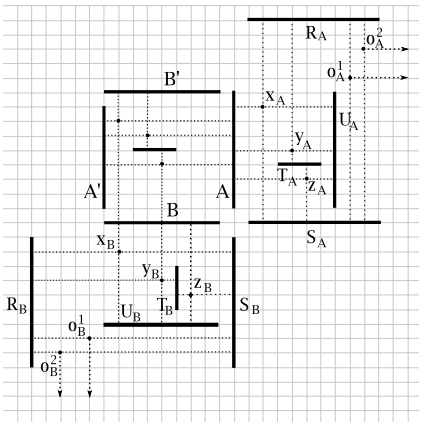

Figure 3: An embedding of an $(A, 2, B, 2)$-variable-box.

Lemma 5 *In any embedding Γ of an (A, B)-perp,*

1. *$\Gamma(B)$ and $\Gamma(B')$ are parallel,*
2. *$\Gamma(A)$ and $\Gamma(B)$ are perpendicular, and*
3. *$\Gamma(A)$ and $\Gamma(A')$ are parallel.*

Definition 6 *A (B, o)-flipper is a bus graph component as shown in Fig. 2.*

Observe that a (B, o)-flipper contains an (A, B)-perp as a subgraph. The dotted arrows in Fig. 2 depicts edges connecting other components of the overall graph.

Lemma 7 *Let i be a $\mathcal{C}$-vertex, and O be a $\mathcal{B}$-vertex. If i is joined with a (B, o)-flipper by an edge (B, i), and O is joined with the (B, o)-flipper by an edge (O, o), then in any embedding Γ,*

1. *$\Gamma((B, i))$ and $\Gamma((O, o))$ are perpendicular, and*
2. *$\Gamma(B)$ and $\Gamma(O)$ are perpendicular.*

Definition 8 *An (A, k, B, l)-variable-box is a bus graph component that contains an (A, B)-perp and $2k$ connectors leaving the component, as shown in Fig. 3*

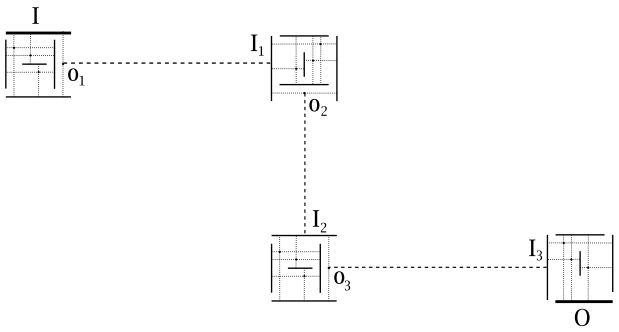

Figure 4: An embedding of an (I, O)-chain.

Lemma 9 *Let (O_A^i, o_A^i) for $i = 1, 2, \ldots, k$ and (O_B^j, o_B^j) for $j = 1, 2, \ldots, l$ be edges joined with an (A, k, B, l)-variable-box. Then in any embedding Γ,*

1. *$\Gamma((O_A^i, o_A^i))$ and $\Gamma(A)$ are perpendicular for any $i = 1, 2, \ldots, k$.*
2. *$\Gamma((O_B^i, o_B^i))$ and $\Gamma(B)$ are perpendicular for any $i = 1, 2, \ldots, l$.*

Definition 10 *An (I, O)-chain is a bus graph component consisting of (I_1, o_1)-flipper, (I_2, o_2)-flipper, (I_3, o_3)-flipper, and an (I_3, O)-perp, as shown in Fig. 4.*

Lemma 11 *In any embedding Γ of an (I, O)-chain, $\Gamma(I)$ and $\Gamma(O)$ are parallel.*

Finally, we are ready to give the transformation from NAE-3SAT to BGR. Let ϕ be an instance of NAE-3SAT, consisting of boolean variables $x_1, \ldots, x_n$, and clauses $C_1, \ldots, C_m$. Construct a bus graph G as follows.

1. For each boolean variable x_i, create a $(X_i, t_i, \overline{X}_i, f_i)$-variable-box, where t_i and f_i are the numbers of distinct occurrences of the literals x_i and $\overline{x_i}$, respectively, in ϕ.
2. For each clause $C_q = (x_i^* \vee x_j^* \vee x_k^*)$, where x^* is either x or $\overline{x}$, create
   (a) a $\mathcal{C}$-vertex c_q,
   (b) an $(I_{q,1}, O_{q,1})$-chain, an $(I_{q,2}, O_{q,2})$-chain, and an $(I_{q,3}, O_{q,3})$-chain,
   (c) edges $(O_{q,1}, c_q)$, $(O_{q,2}, c_q)$ and $(O_{q,3}, c_q)$,
   (d) edges $(I_{q,1}, p_i)$, $(I_{q,2}, p_j)$ and $(I_{q,1}, p_k)$, where $p_i = o^r_{X_i}$ if $x_i^* = x_i$ and $p_i = o^r_{\overline{X}_i}$ if $x_i^* = \overline{x_i}$, and it is the rth occurrence of x_i^* being considered.

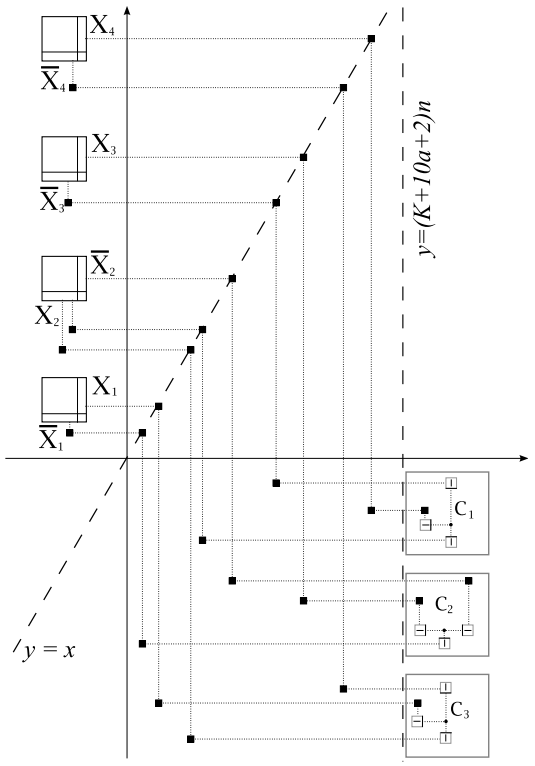

Figure 5: A schematic embedding of G, where ϕ consists of the clauses $C_1 = (x_2 \vee \overline{x_3} \vee x_4)$, $C_2 = (\overline{x_1} \vee \overline{x_2} \vee x_3)$,and $C_3 = (x_1 \vee x_2 \vee \overline{x_4})$ with a satisfying truth assignment $x_1 = x_3 = x_4 =$ true and $x_2 =$false. Note the regions separated by the dashed lines and $x-, y-$axes.

Since every gadget is of linear size, the transformation clearly takes polynomial time. Finally, the following lemma completes the proof of Theorem 1.

Lemma 12 *$\phi \in$ NAE-3SAT if and only if $G \in$ BGR.*

Proof Sketch: Suppose $\phi \in$ NAE-3SAT. An embedding Γ of G can be constructed as shown in Fig. 5. Note that the variable boxes are embedded so that the buses corresponding to true (false) literals literals are drawn vertically (vertically, resp.).

Now, suppose $G \in$ BGR, and take an embedding Γ of G. By Lemma 5, $\Gamma(X_i)$ is perpendicular to $\Gamma(\overline{X}_i)$ for each variable box, so assign each variable x_i to be true if $\Gamma(X_i)$ is vertical and false otherwise. To see that this truth-assignment satisfies the clauses, consider a clause $C_q = (x_i^* \vee x_j^* \vee x_k^*)$. The clause vertex c_q is adjacent to three buses $O_{q,1}$, $O_{q,2}$, and $O_{q,3}$ at the end of (I, O)-chains. Since c_q can be joined to at most two parallel buses, at least one of these three buses must be drawn horizontally, and at least one must be drawn vertically. Take any one of the three buses, say $O_{q,1}$, and consider the literal bus to which $O_{q,1}$ connects in the variable box. By Lemmas 9 and 11, the orientation of these two

buses must be the same. This implies that the clause vertex c_q is connected to at least one vertical literal bus, and at least one horizontal literal bus. Thus, the truth-assignment satisfies ϕ. □

4 Variations of Bus Graph Realizability

We now look at variations of the BGR problem. In the original BGR problem stated in Sect. 1, each $\mathcal{C}$-vertex has a maximum degree of 4, due to the orthogonal drawing style. Analogous problems can be devised for the class of bus graphs where the maximum degree of the $\mathcal{C}$-vertices is either 2 or 3. First, consider the class of bus graphs where the $\mathcal{C}$-vertices have maximum degree 1. These graphs are trivially realizable by simply drawing all the buses along a grid line. However, if the maximum degree of $\mathcal{C}$-vertices is greater than or equal to 2, the problem becomes harder. The next result can be shown by a similar transformation based on gadgets using $\mathcal{C}$-vertices with bounded degree.

Theorem 13 *BGR is NP-complete when the maximum degree of $\mathcal{C}$-vertices is 2 or 3.*

In order to realize a given bus graph, one must decide the orientations of the buses. Since a connector can be joined to at most two horizontal buses and at most two vertical buses, all realizable bus graphs admit a bipartition of buses by orientation. As the following results suggests, even deciding whether the buses can be properly oriented is hard.

BUS-ORIENTATION Instance: A bipartite graph $G = (\mathcal{B}, \mathcal{C}; \mathcal{E})$ such that $\forall c \in \mathcal{C}$, $deg(c) \leq 4$.

Question: Can $\mathcal{B}$ be partitioned into two disjoint sets $\mathcal{B}_\mathcal{H}$ and $\mathcal{B}_\mathcal{V}$, such that $\forall c \in \mathcal{C}$, c is adjacent to no more than two vertices in $\mathcal{B}_\mathcal{H}$ and no more than two vertices in $\mathcal{B}_\mathcal{V}$?

Theorem 14 *BUS-ORIENTATION is NP-complete.*

Finally, we study a variation (BGR+BL) of BGR in which the lengths of buses are given as input. The following result is due to a transformation from the SET-PARTITION [3] problem.

Theorem 15 *BGR+BL is NP-hard. It is also NP-hard if the maximum degree of $\mathcal{C}$-vertices is 2, or if we require the buses to be parallel to each other.*

5 Concluding Remarks and Open Problems

Although bus graph realizability is an NP-complete problem, some special classes of graphs admit polynomial time solutions. For example, if the given bus graph G is a tree, G *always* admits a bus graph embedding. What other classes of graphs admit efficient recognition algorithms for realizability is open.

One may search for approximate solutions to these problems. It is unclear, however, what optimization criteria would be used. With applications in VLSI in mind, one may wish to lay out all the buses first, and then maximize the connectivity by maximizing the number of connectors realized in the layout.

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