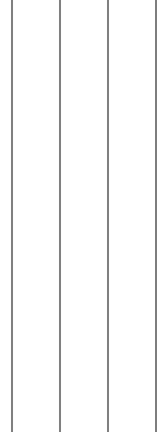


## Multiple Wire Circuit Representation

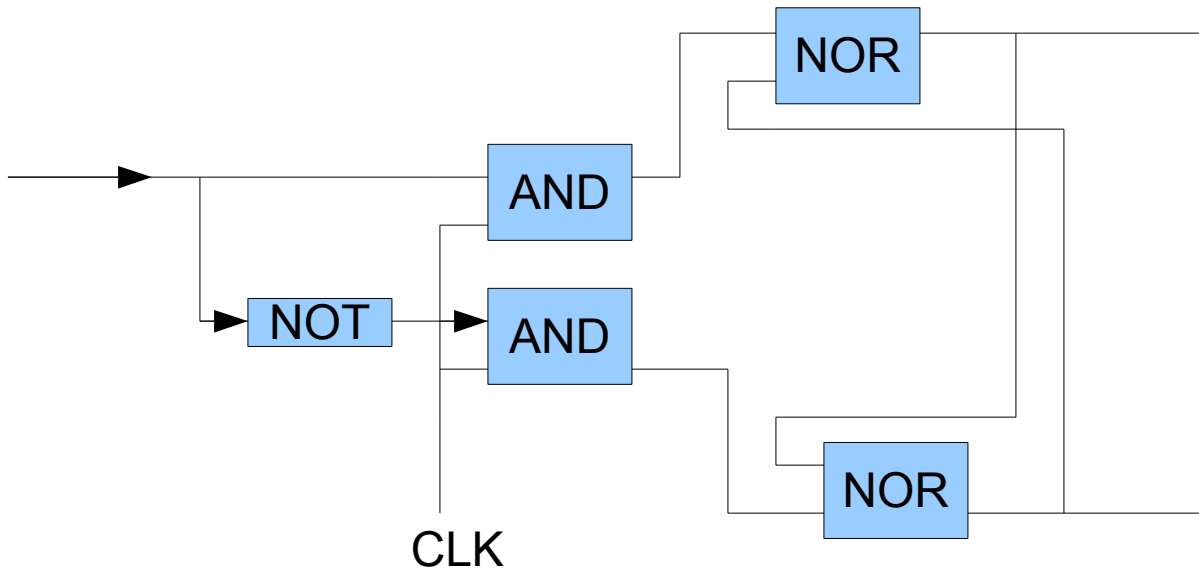


## Multiple Wire Black Box Representation

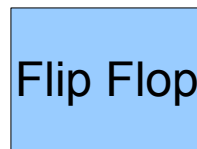


2.1.3 FETCH HARDWARE CIRCUIT DIAGRAMS

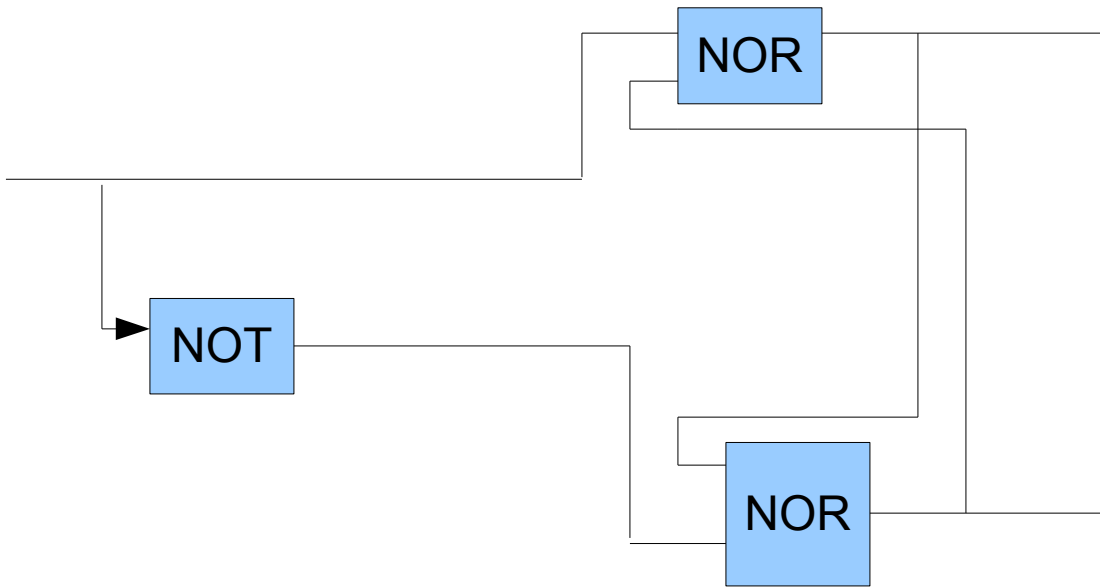
Normal Register



Normal Register Black Box Representation



# Continuous Stream Register



## Continuous Stream Register Black Box Representation



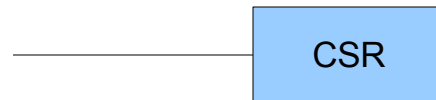
## Intermediate View of a Generic 1-Bit Register



### List of Major 1-Bit Registers

- BZO Reg
- Math Reg
- Internal R/W Reg
- R/W Reg
- B Reg
- is-Zero? (iZ)
- Overflow? (Ov)

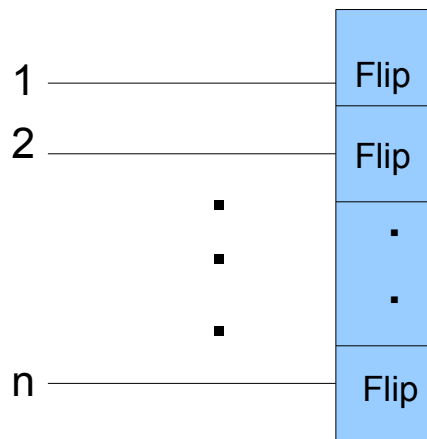
## Intermediate View of a Continuous Stream Register



### List of Major 1-Bit CS Registers

- WAM Reg
- ON/OFF Reg

Intermediate view of an n-Bit register with a single thick wire input.



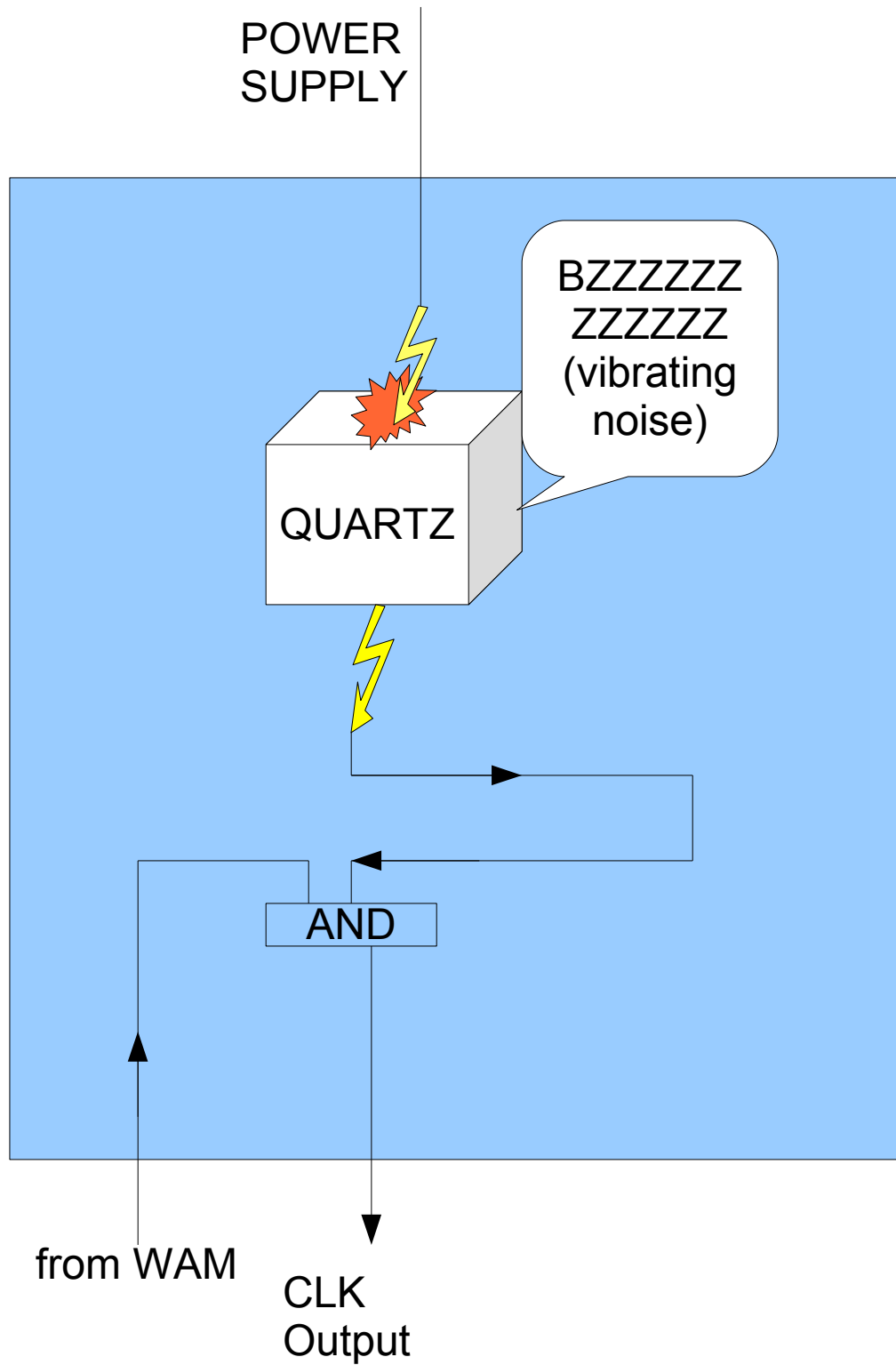
Black Box Representation of an n-Bit register receiving input from a single thick wire



### List of Major (Non-trivial) Registers

- PC Counter
- RIGHT Reg
- LEFT Reg
- iZBiz (5 Bit) Reg
- CMS (3 Bit) Reg (also C, M, S)
- Stb (Stable) Reg (0)
- Mem. Reg
- ALU Reg
- IR (8 Bit) Reg
- R-0 Reg
- R-1 Reg
- A-Out Reg

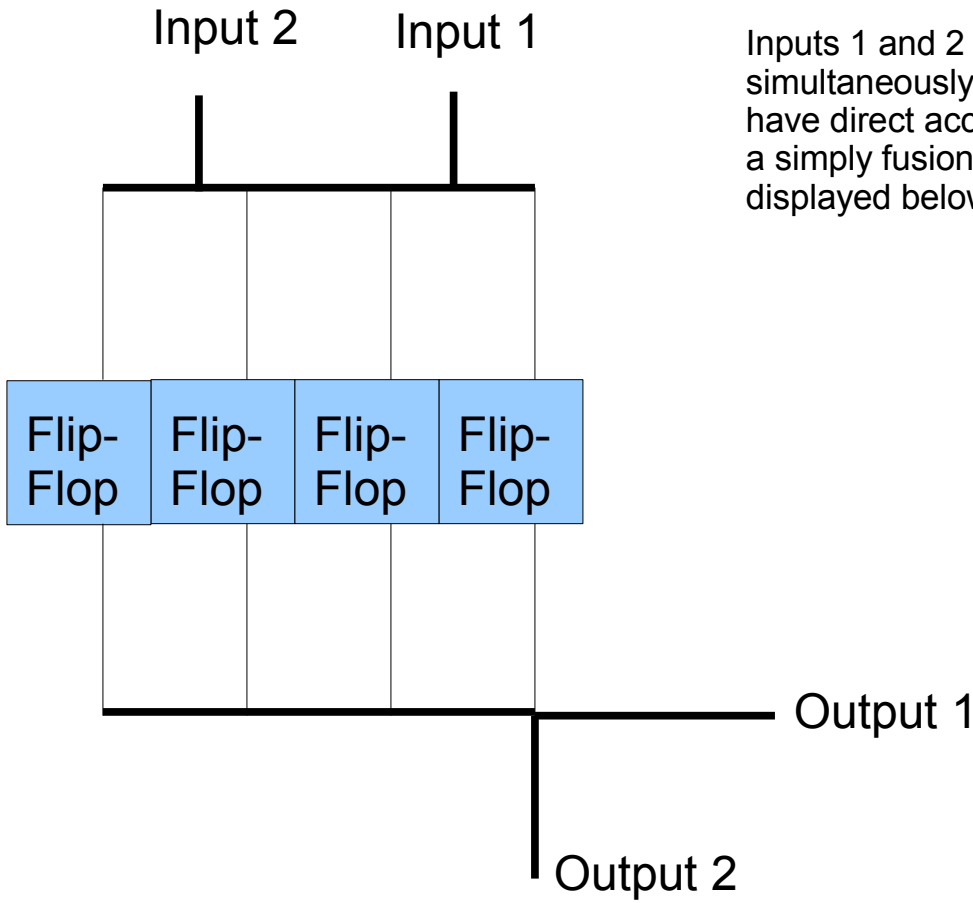
# In-depth view of the GDK Clock



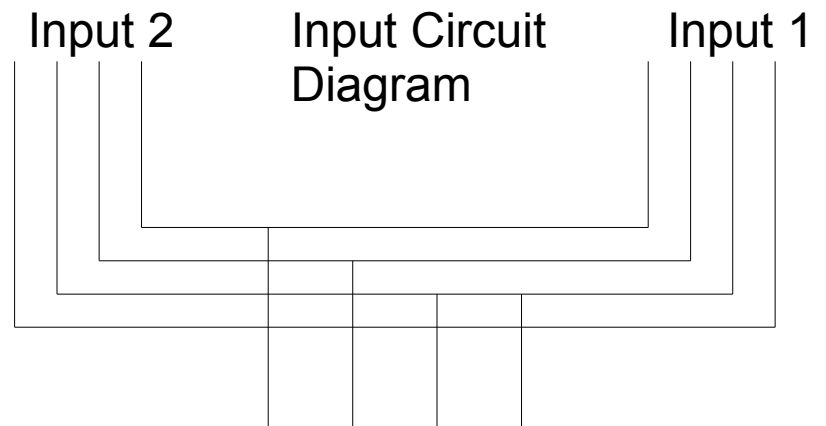
Clock Black Box Representation



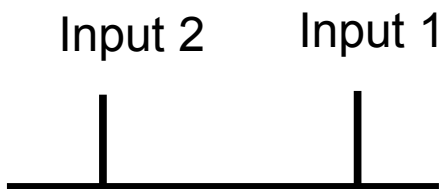
# Intermediate view of the PC counter



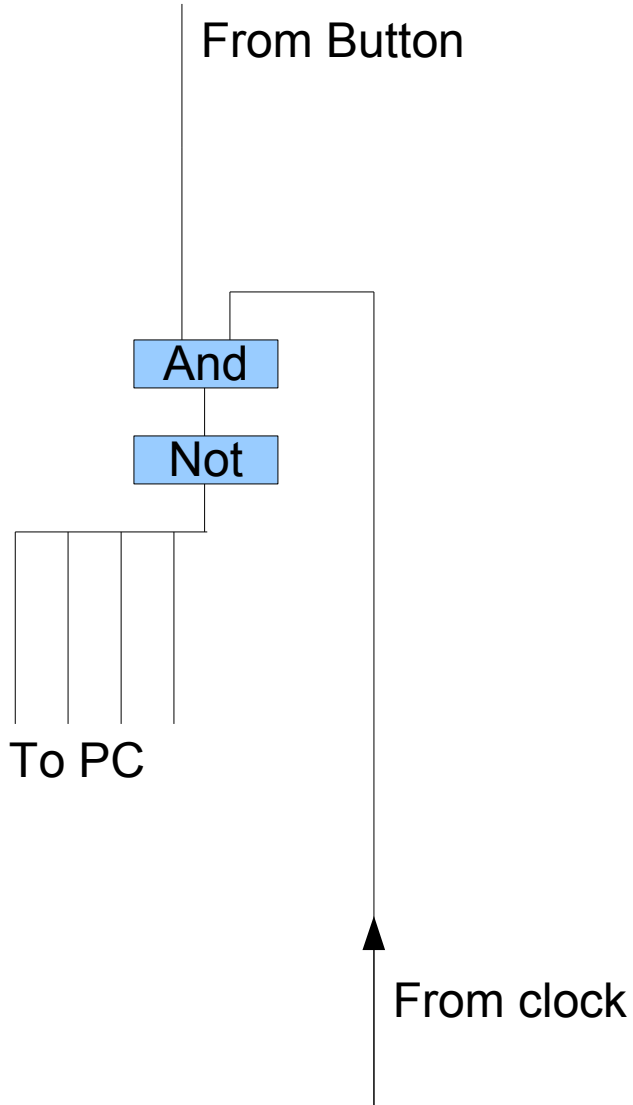
Inputs 1 and 2 will never simultaneously hold information. They have direct access to each bit through a simple fusion of their wires as displayed below.



Input Black Box Representation



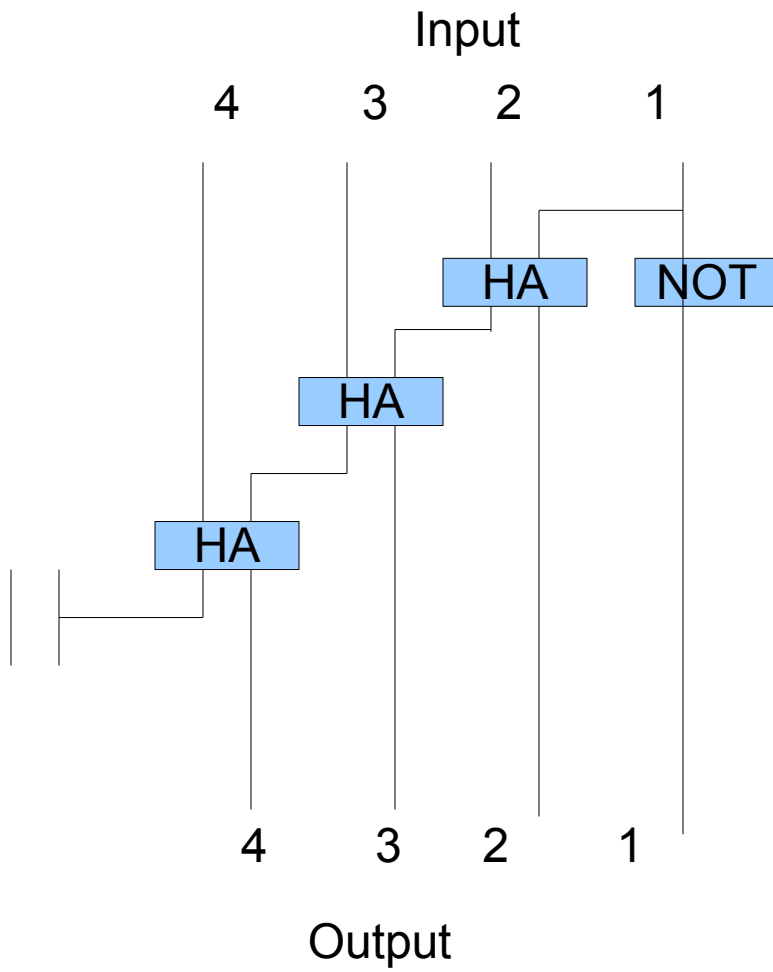
# PC (Zero) Initializer Circuit Diagram



PC Initializer Black Box Representation (Two 1-Bit inputs, One 4-Bit output (all zeros))



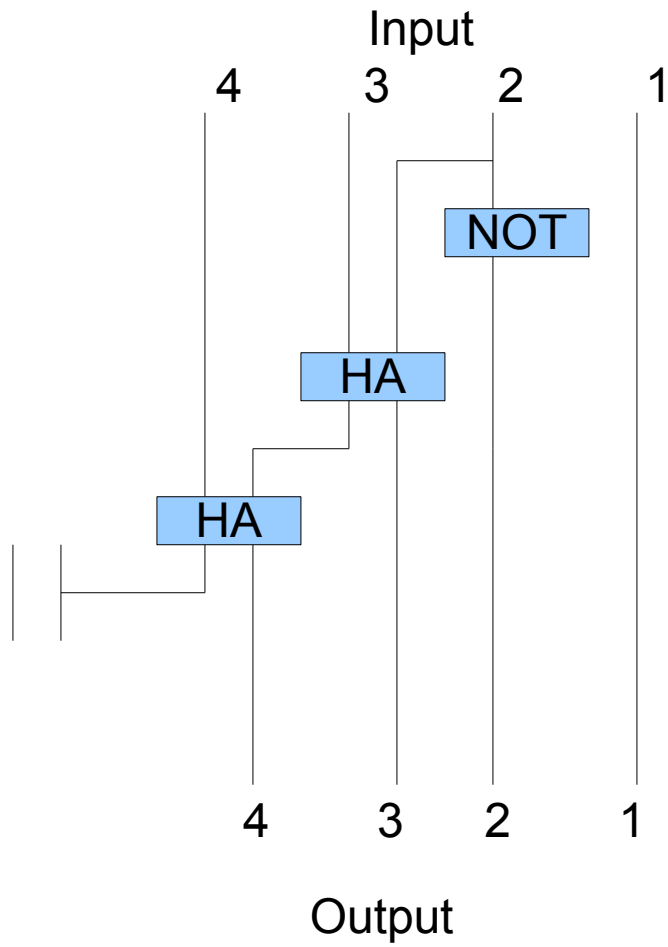
# UNIT ADDER ALU -- Circuit Diagram



## UNIT ADDER ALU – Black Box Representation

UAA

# TWO UNIT ADDER ALU

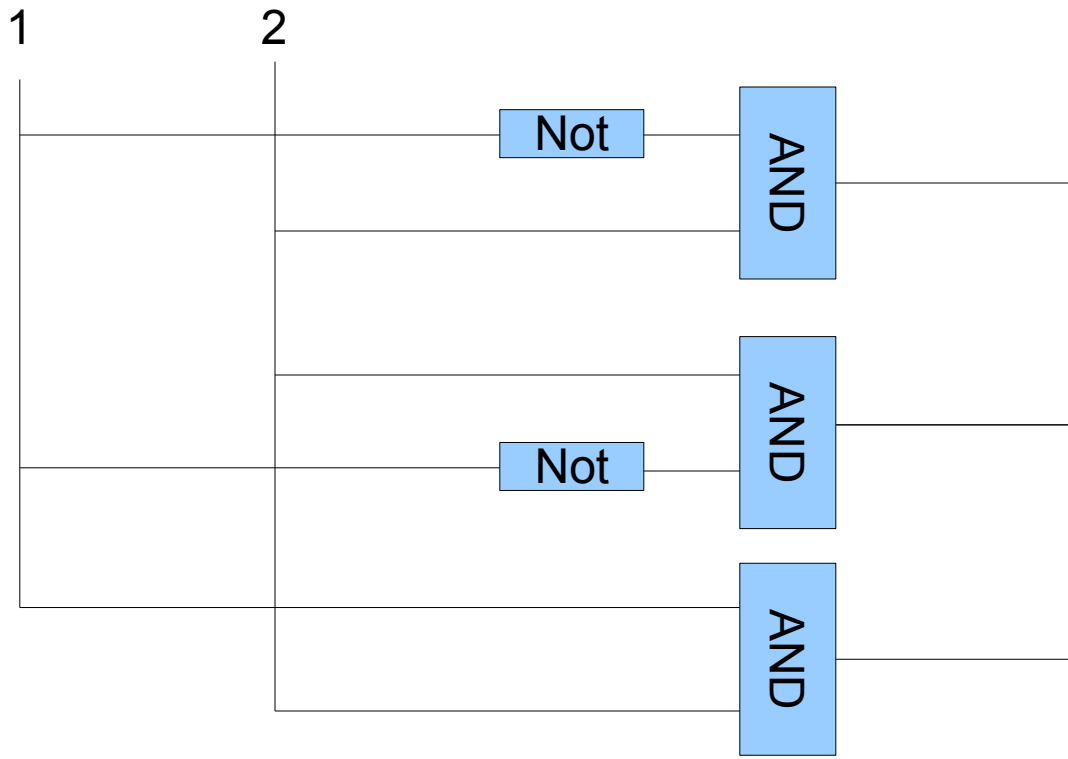


TWO UNIT ADDER ALU – Black Box Representation

UAA(2)



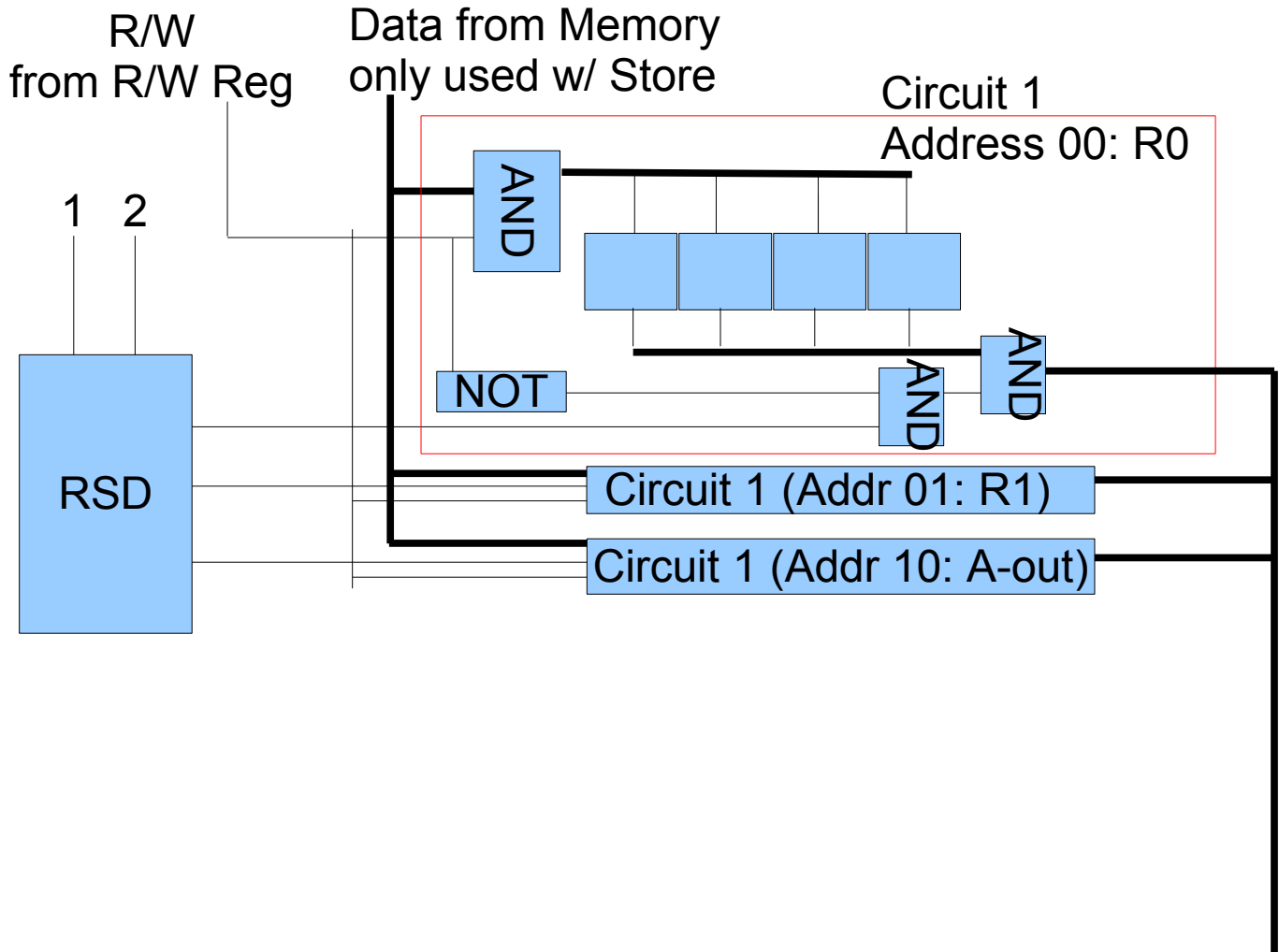
# Register Selection Device (RSD)



RSD Black Box (2 inputs, 3 outputs)



# Register Data Retriever

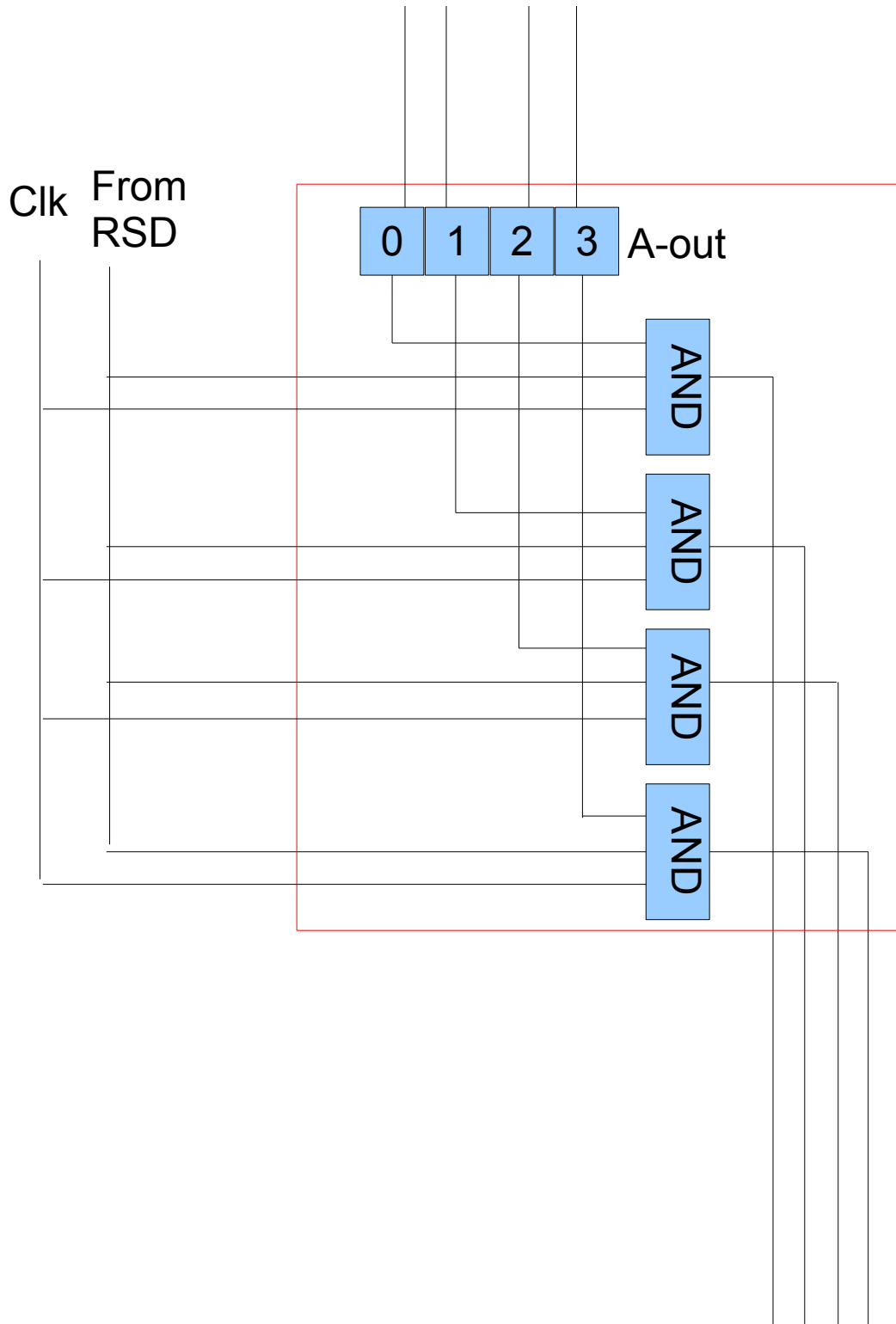


Register Data Retriever (3 inputs and clock, 4 bit output)

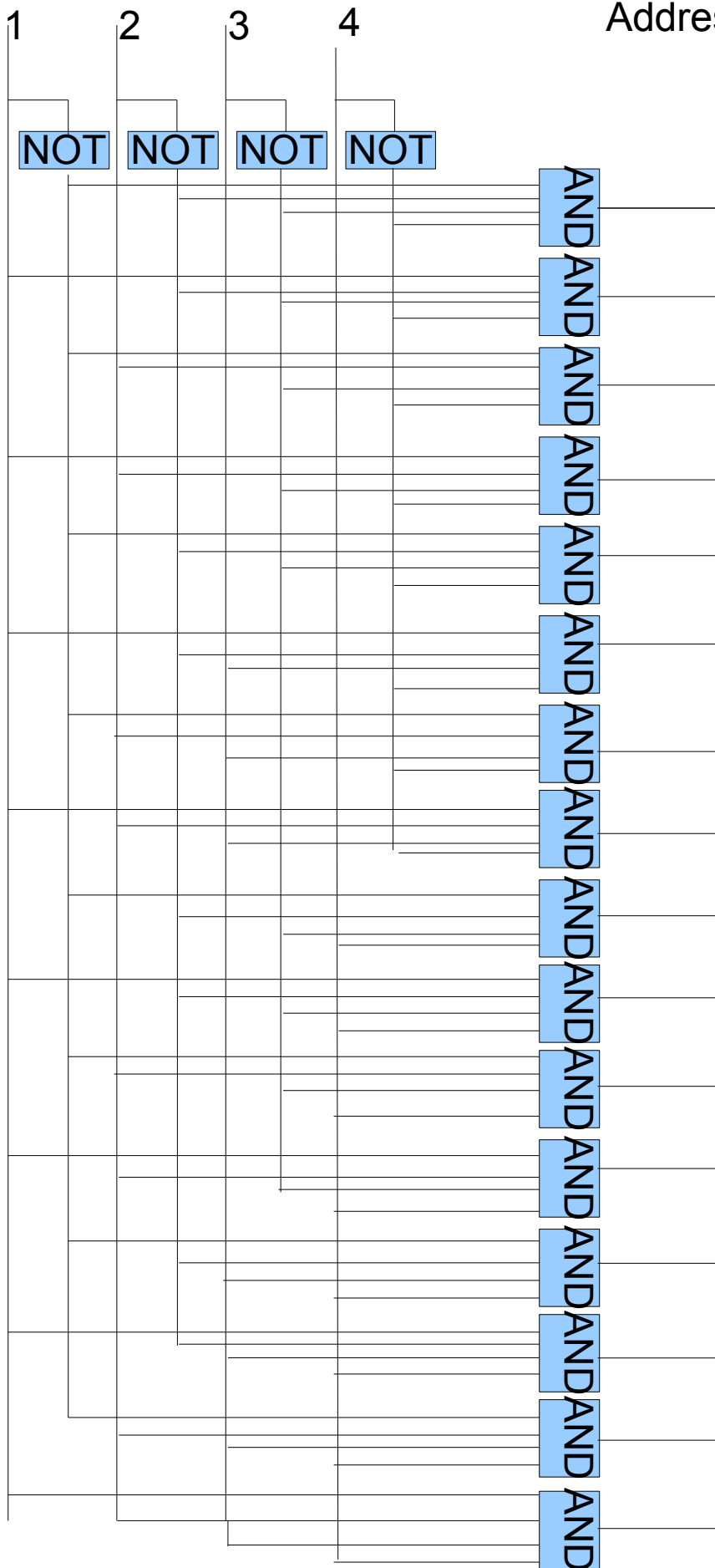


# Circuit 1 in Detail for A-Out Register

From ALU Reg



# Address Selection Device (ASD)



ASD Box (4 inputs, 16 outputs)

ASD

# RAM Circuit Diagram

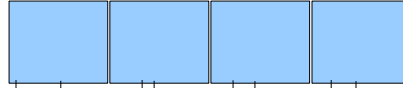
Address 1  
from PC

Address 2  
from PC

ASD

ASD

Circuit 1 Address 0000



AND  
AND

Circuit 1 (0001)

Circuit 1 (0010)

Circuit 1 (0011)

Circuit 1 (0100)

Circuit 1 (0101)

Circuit 1 (0110)

Circuit 1 (0111)

Circuit 1 (1000)

Circuit 1 (1001)

Circuit 1 (1010)

Circuit 1 (1011)

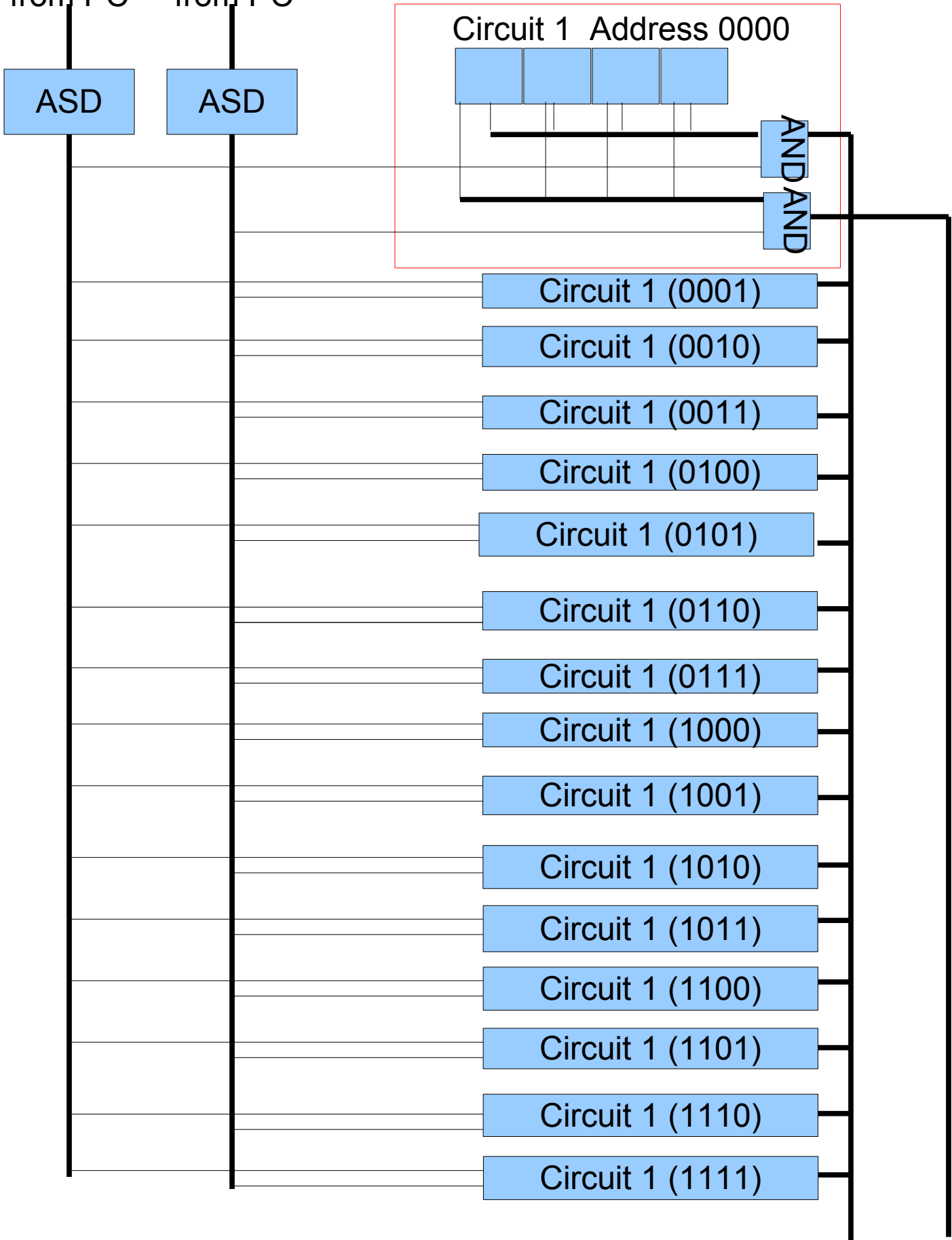
Circuit 1 (1100)

Circuit 1 (1101)

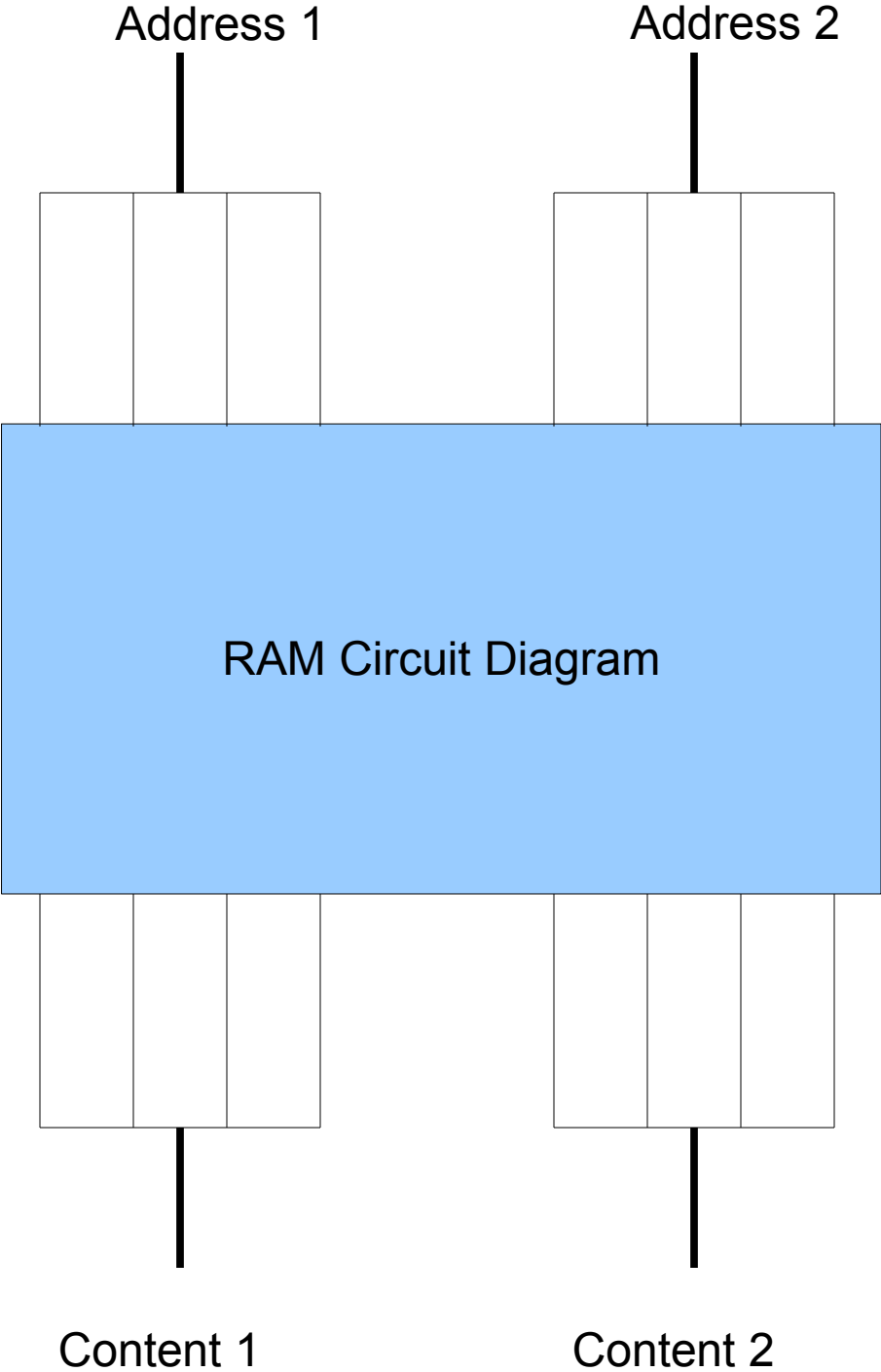
Circuit 1 (1110)

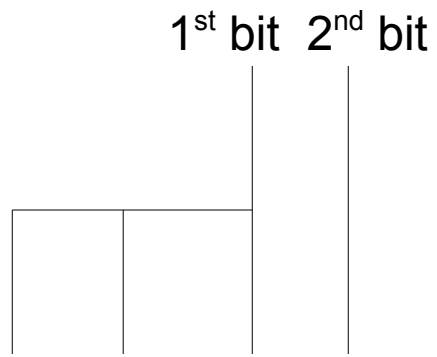
Circuit 1 (1111)

To IR 0-3 To IR 4-7

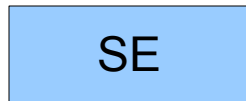


# RAM Circuit Diagram Black Box



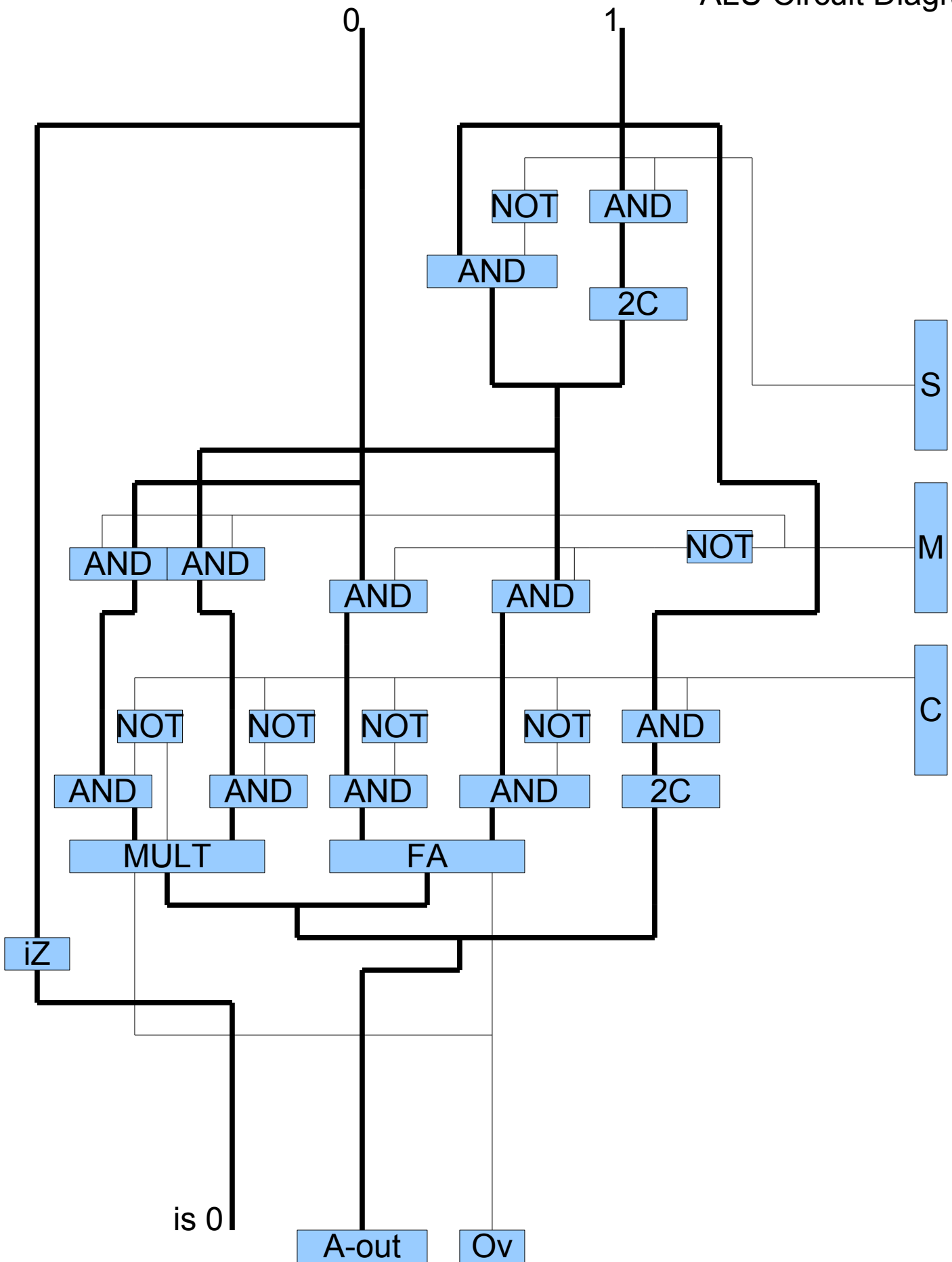


Sign Extend Box-2bits to 4 bits (2 input, 4 output)



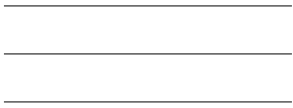
2.3.3A-OUT UPDATE PHASE 1CIRCUIT DIAGRAMS

ALU Circuit Diagram



# CMS 3 Wire Circuitry

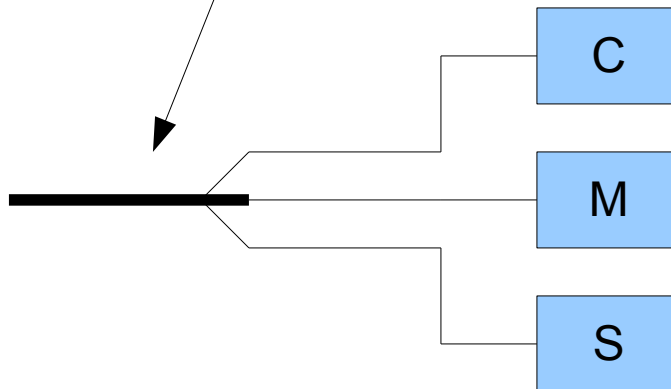
3-Bit wire circuitry



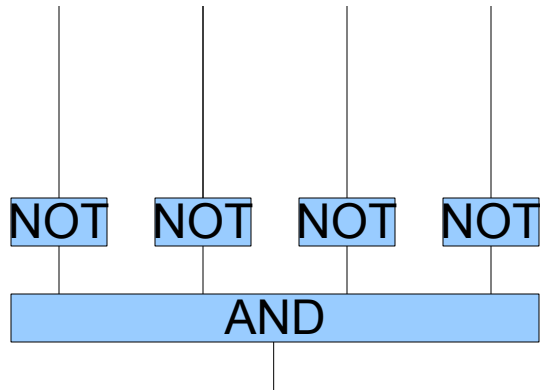
3-Bit wire black box representation



Intermediate view of the C | M | S register



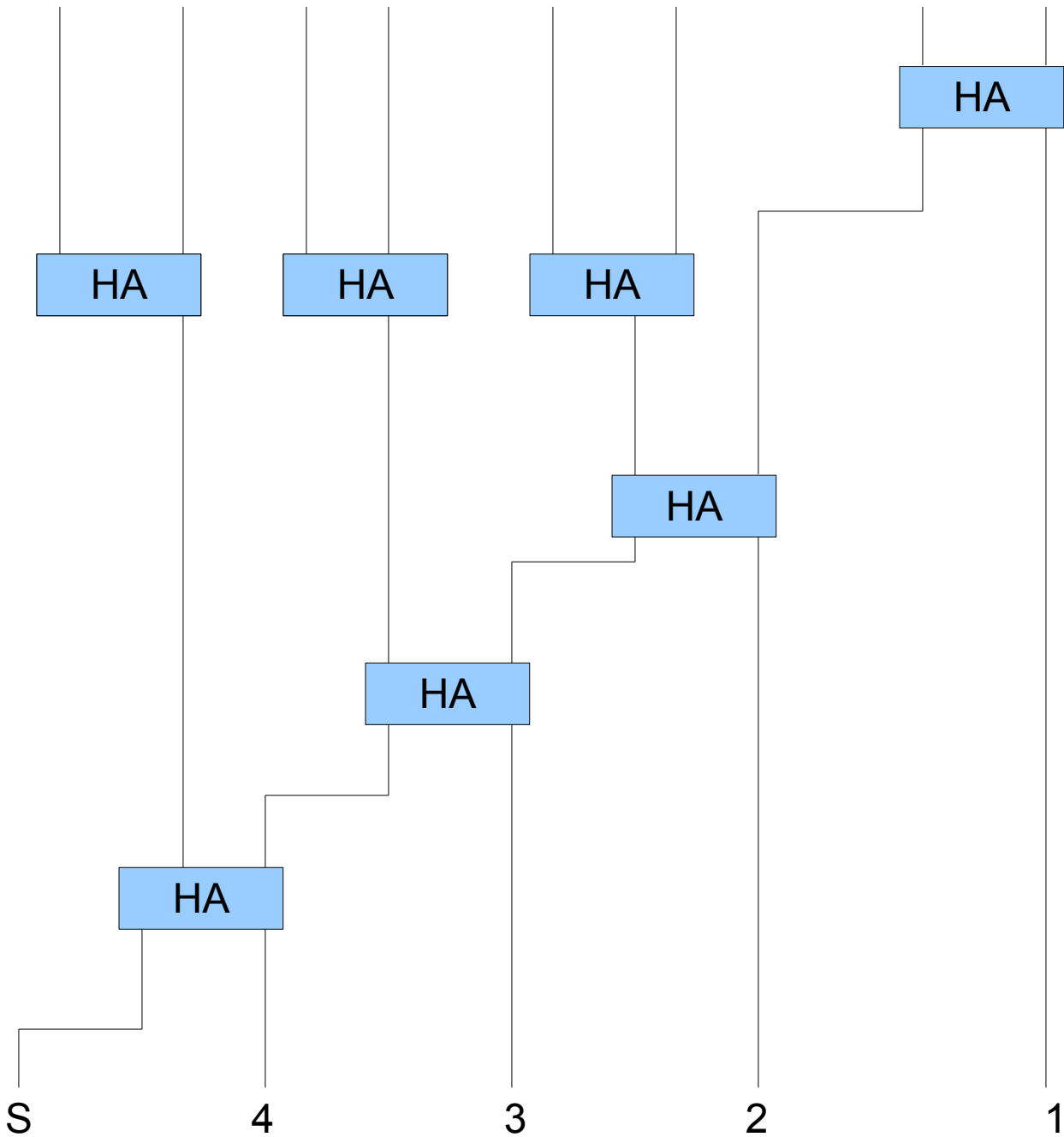
## Is Zero Box – Circuit Diagram



is Zero Box – Box Representation



# FULL ADDER CIRCUIT DIAGRAM

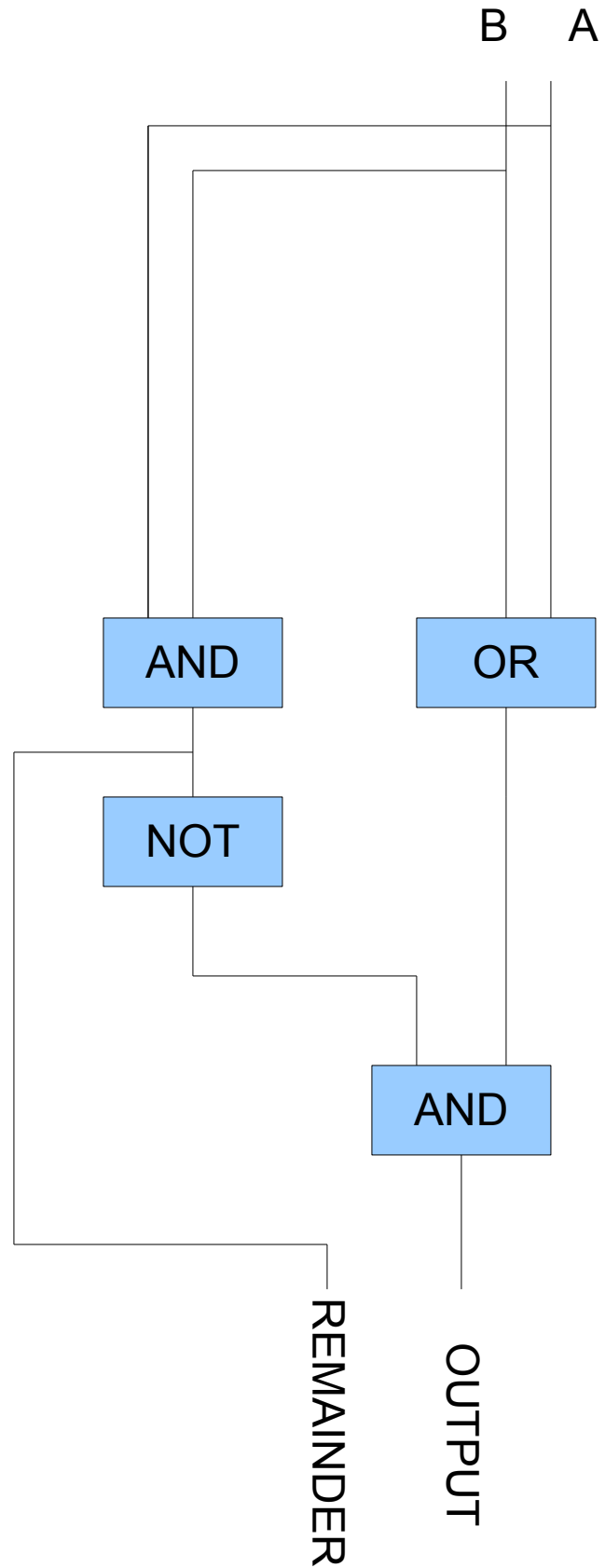


## FULL ADDER BLACK BOX REPRESENTATION 2



# HALF ADDER CIRCUIT DIAGRAM

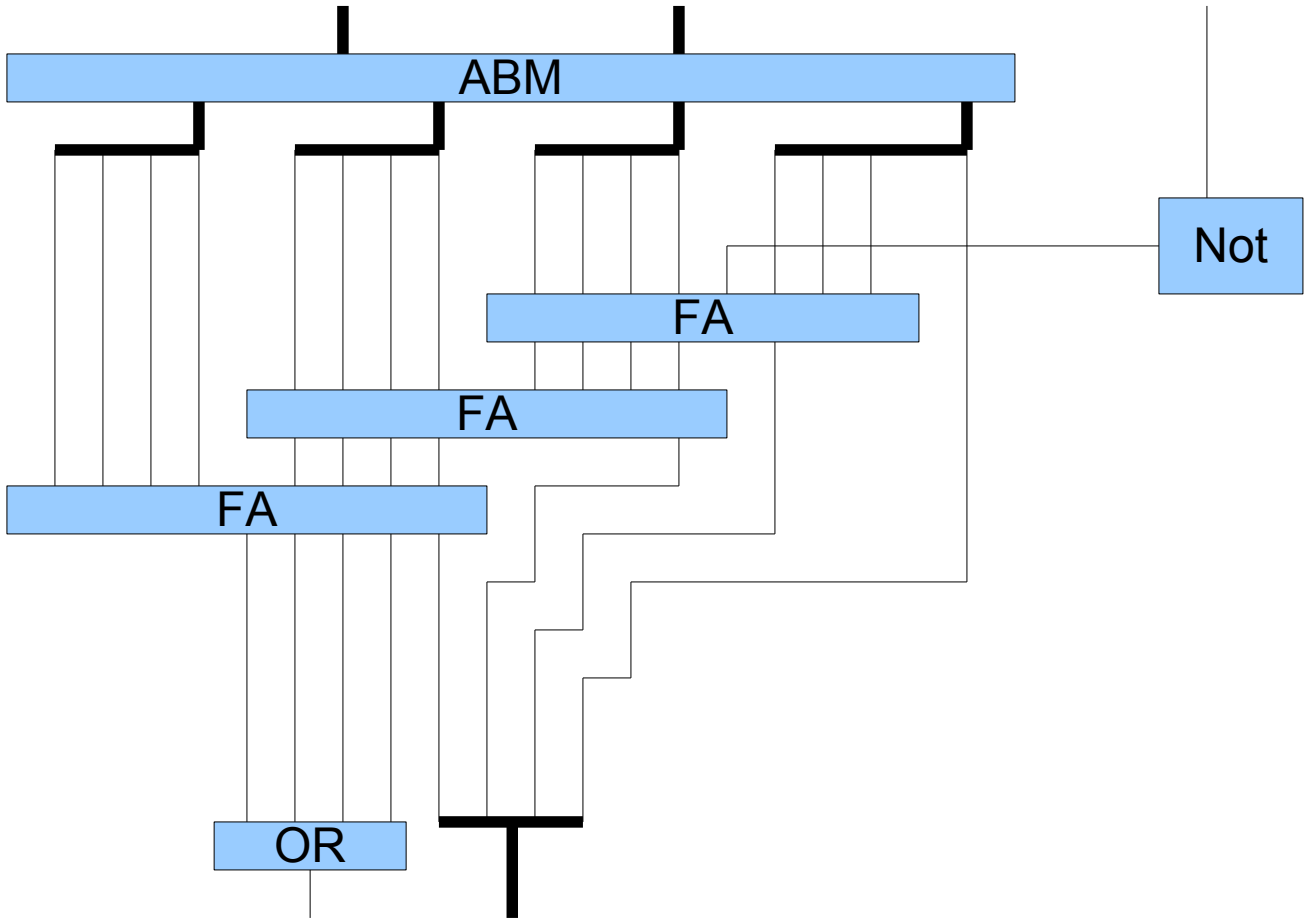
AND unkeyed



BLACK BOX  
REPRESENTATION

HA

# Multiplication Circuit Diagram

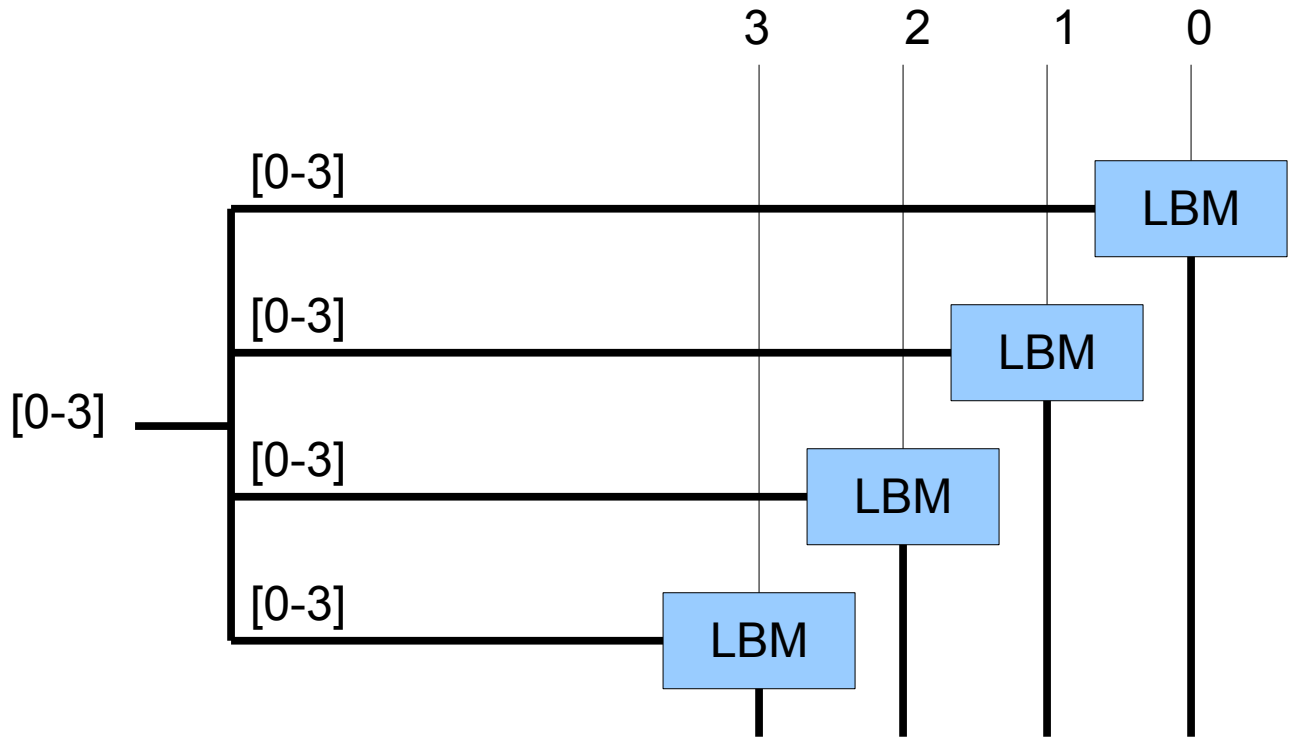


## Multiplication Box Representation

(2 4-Bit and one binary 1 input, 1 4-Bit and one Overflow bit output)

MULT

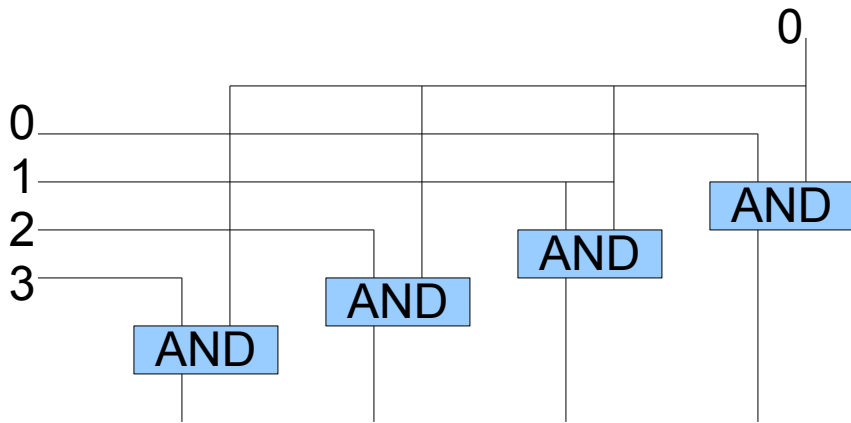
# All Bits Multiplication Box Circuit Diagram



All Bits Multiplication Box Box Diagram (2 4-bit inputs, 4 4-bit outputs)

ABM

# Left Bit Multiplication Box Circuit Diagram

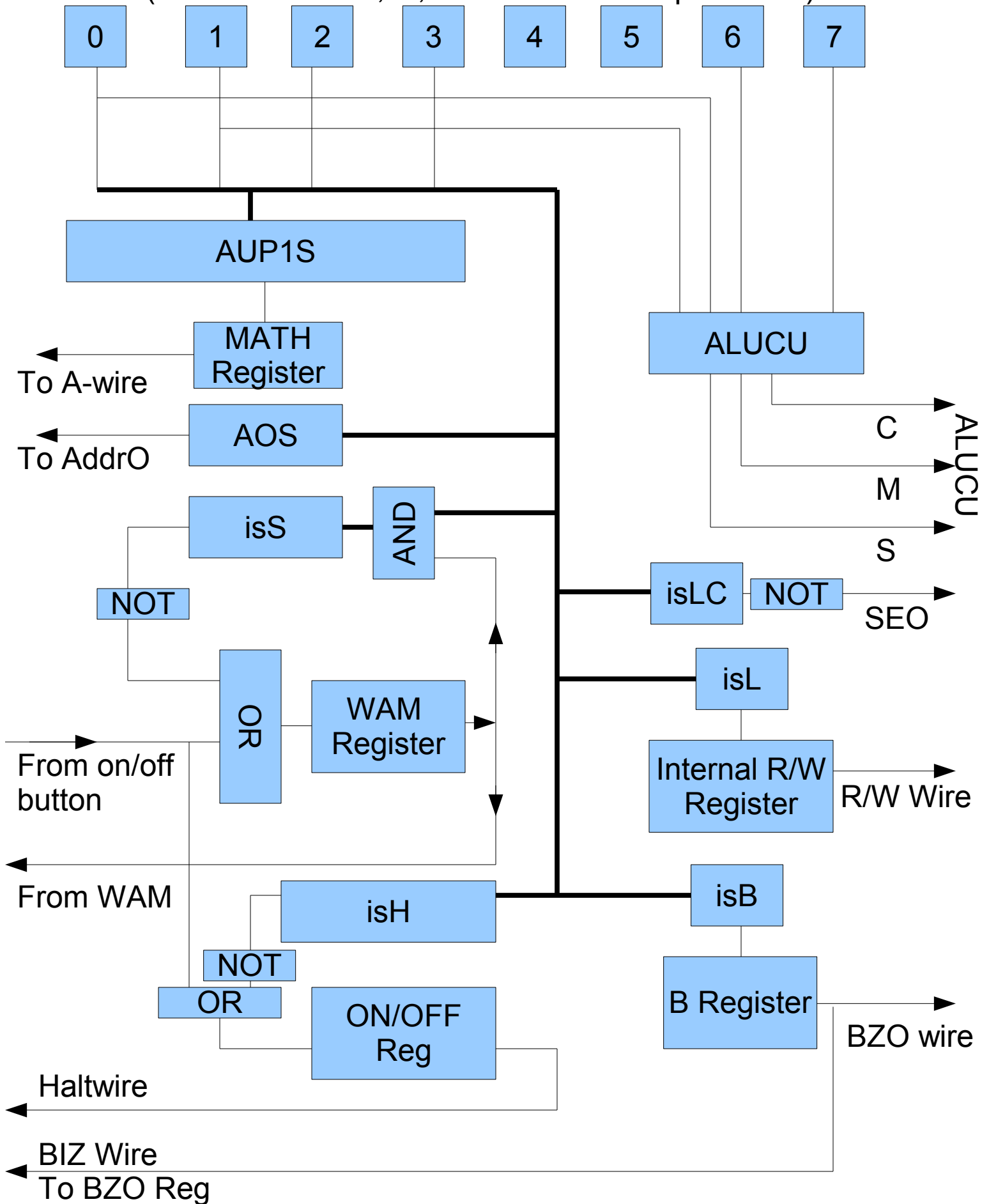


# Left Bit Multiplication Box Box Representation

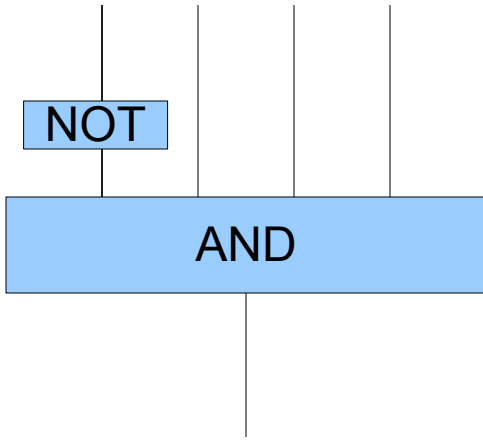


8 bit OP-CODE from IR

(each box is a bit, ie, box 0 is the bit at position 0)



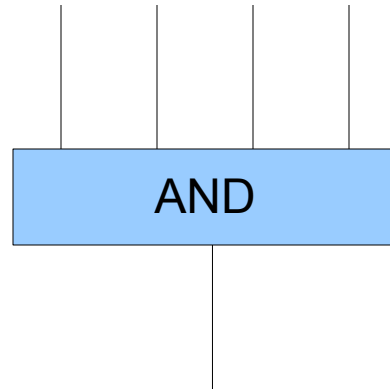
is Stop (checks if the operation is Stop)



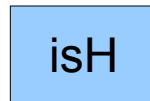
isStop Black Box  
1 if OP-CODE is STOP  
0 for anything else



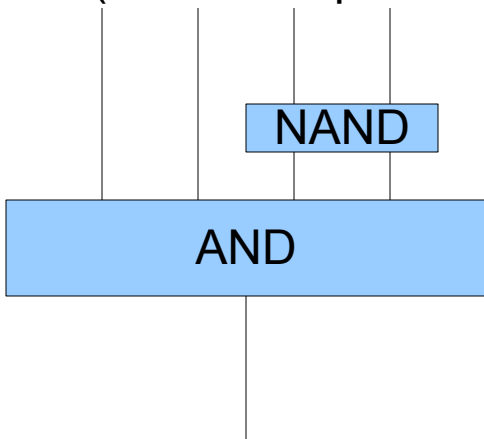
isHalt (checks if operation is Halt)



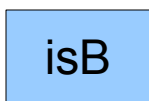
is Halt Black Box  
1 if the OP-CODE is Halt  
0 for anything else



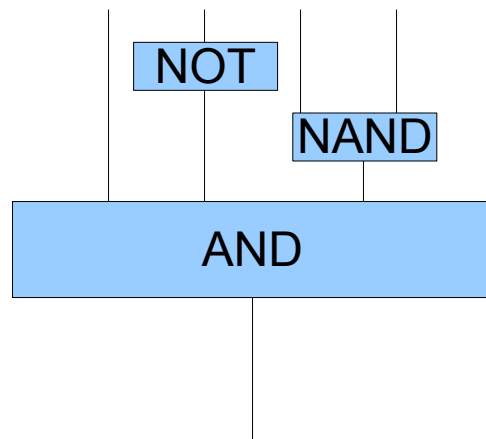
isBiz (checks if operation is Biz)



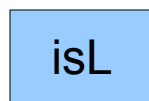
isBiz Black Box  
1 if OP-CODE is BIZ  
0 if anything else



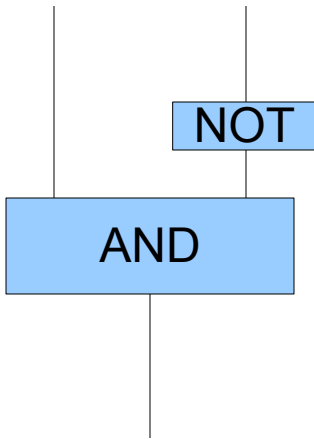
isLoad (checks if operation is LOAD)



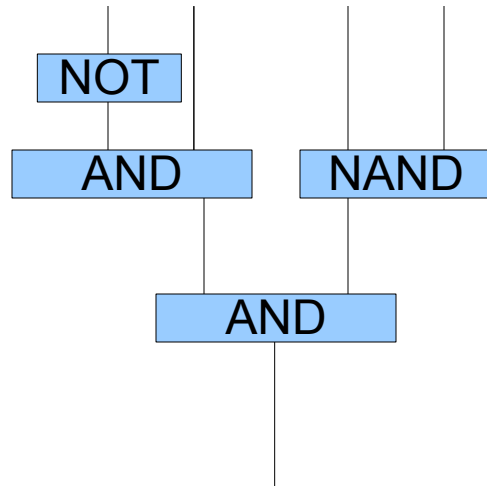
isLoad Black Box  
1 if OP-CODE is LOAD  
0 if anything else



isLoad or Comp  
(checks if operation is LOAD or  
COMP)



is Store (checks if operation is Store)



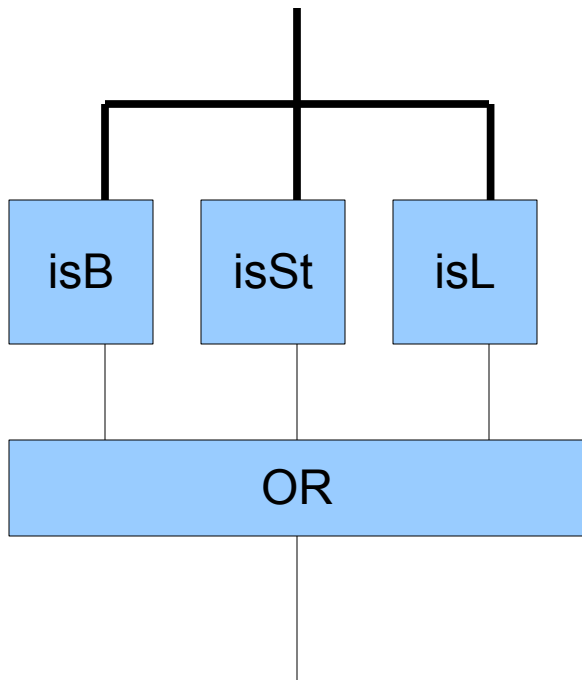
isLoad or Comp Black Box  
1 if OP-CODE is COMP or LOAD  
0 for anything else



isStore Black Box  
1 if OP-CODE is STORE  
0 for anything else

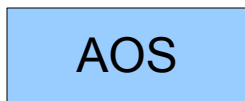


# AddrO Stream Chooser

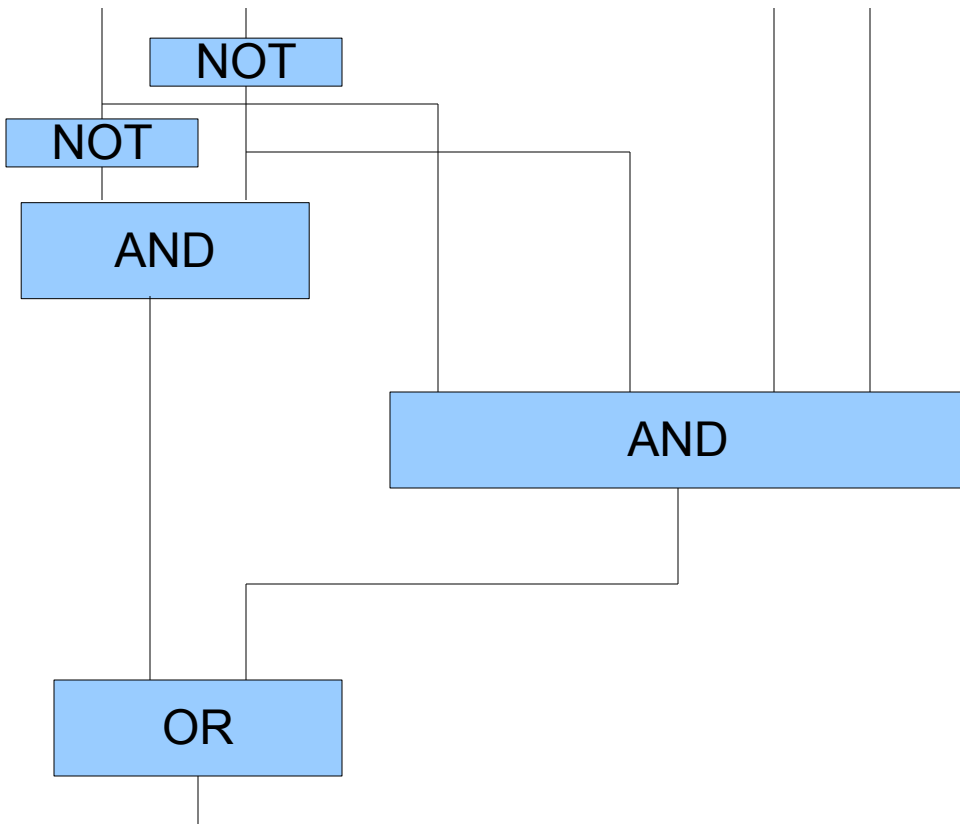


To AddrO  
1 if Address is last 4 bits  
0 if anything else

AddrO Stream (1, 4 bit input, 1 output)



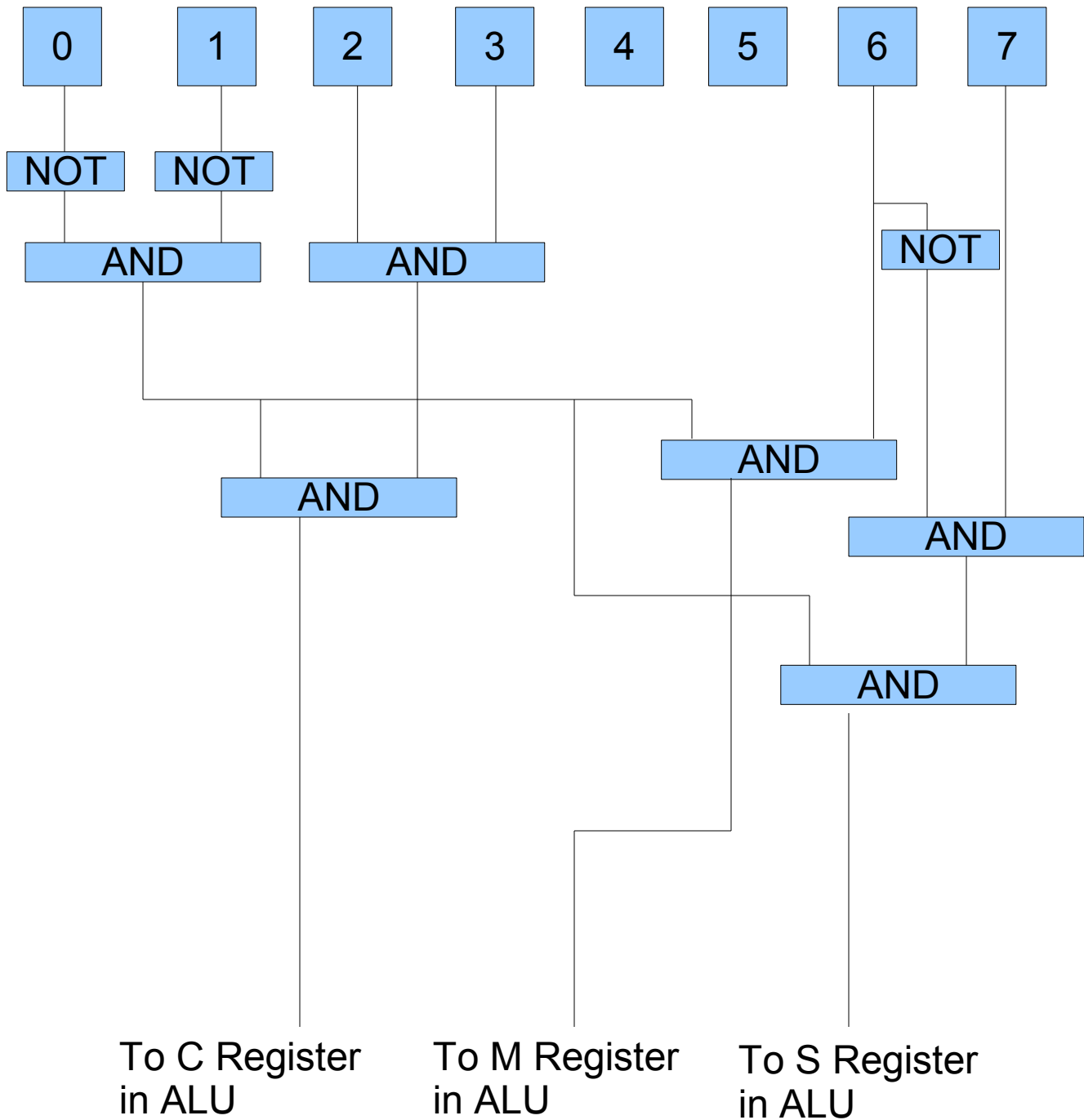
# A-Out Update Phase 1 Selector



A-Out Update Phase 1 Selector (4 inputs-0,1,2,3 bits of OP-CODE, 1 output)

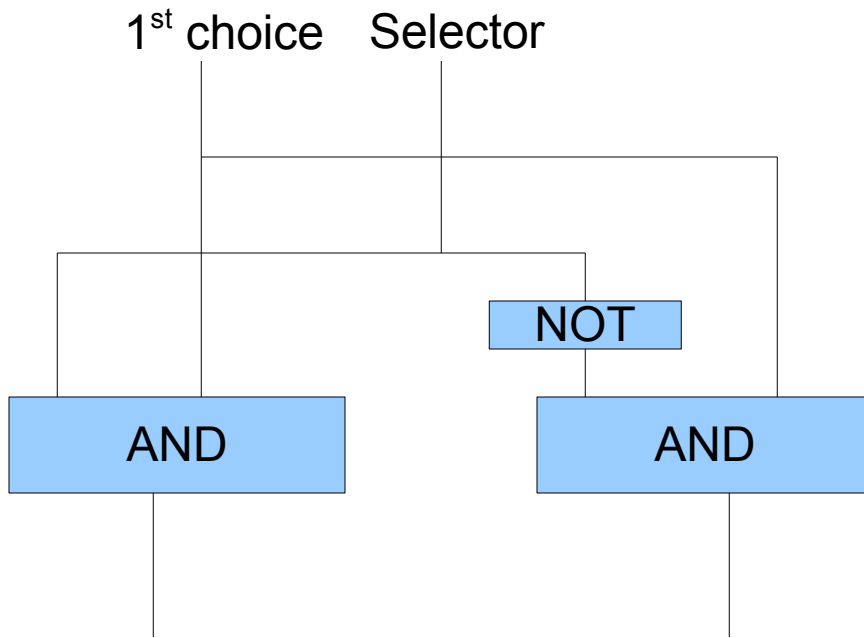
AUP1S

# ALU CU



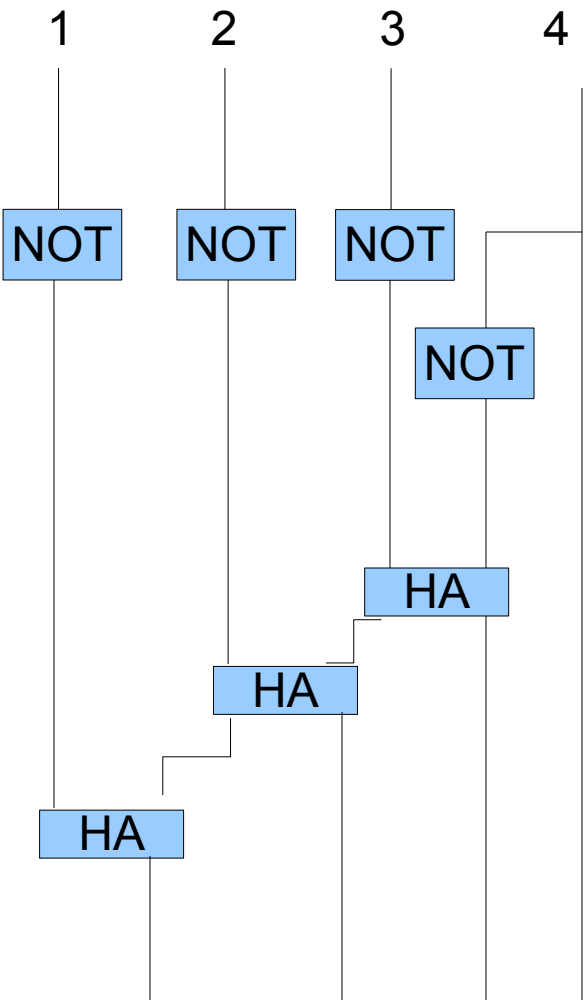
ALU CU Black Box (6 inputs-0,1,2,3,6, and 7 bits of OP-CODE, 3 outputs for C, M, S registers)





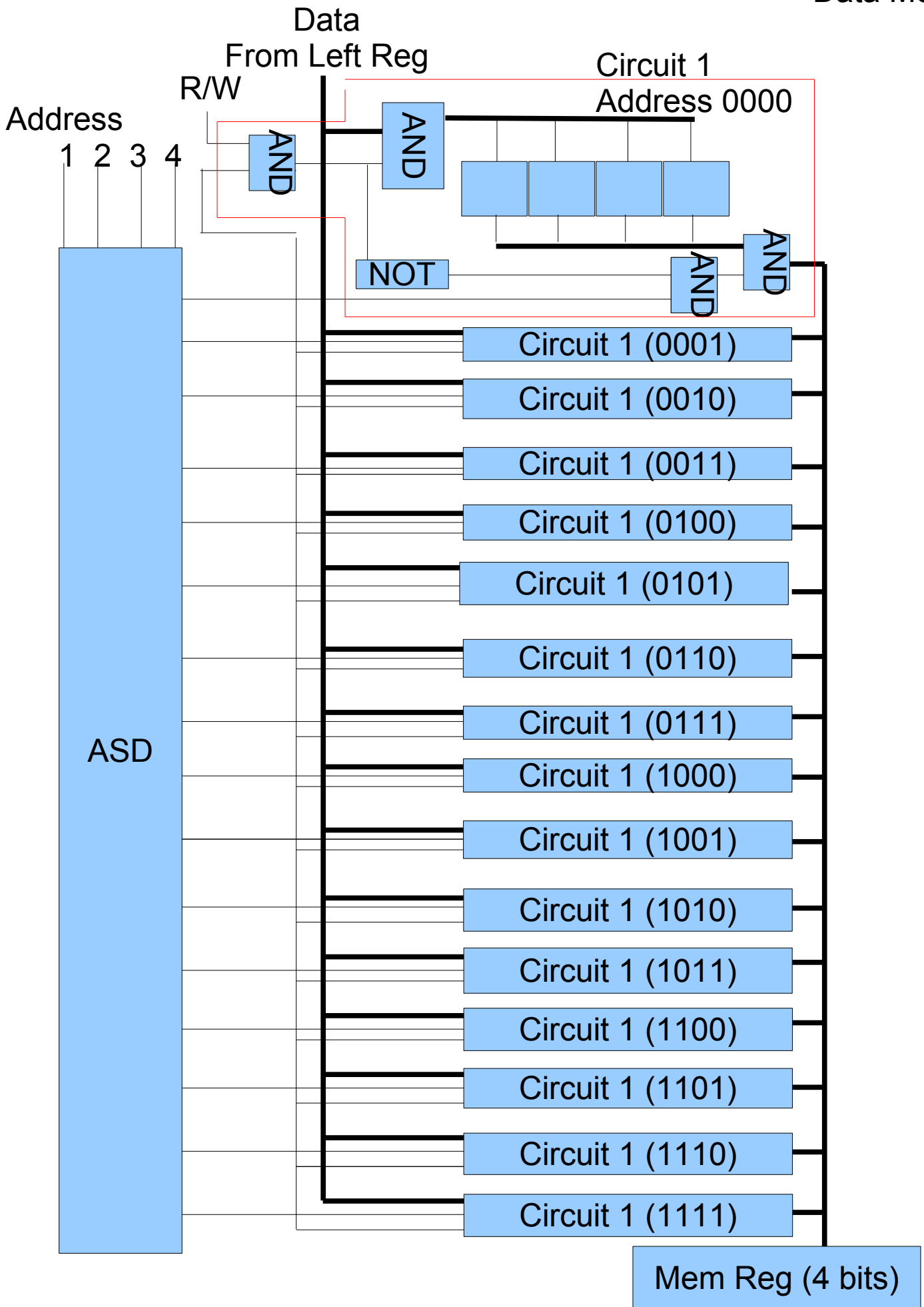
BIZ Selector (1 choice and 1 selector input, 2 outputs)





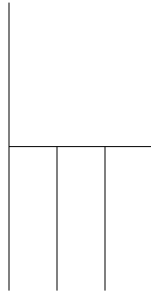
2's Complement Box (4 input, 4 output)



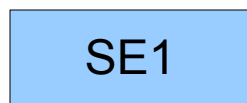


2.4.3 WRITE HARDWARE CIRCUIT DIAGRAMS

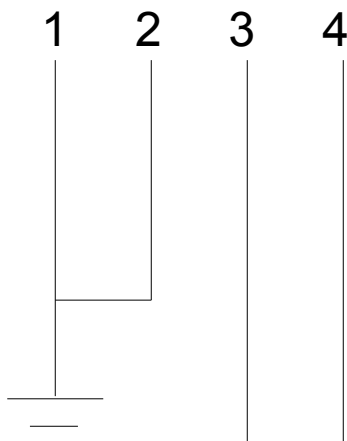
Sign Extend (1 to 4 bits)



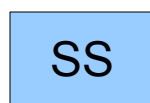
Sign Extend Black Box (1 bit input to 4 bit output)



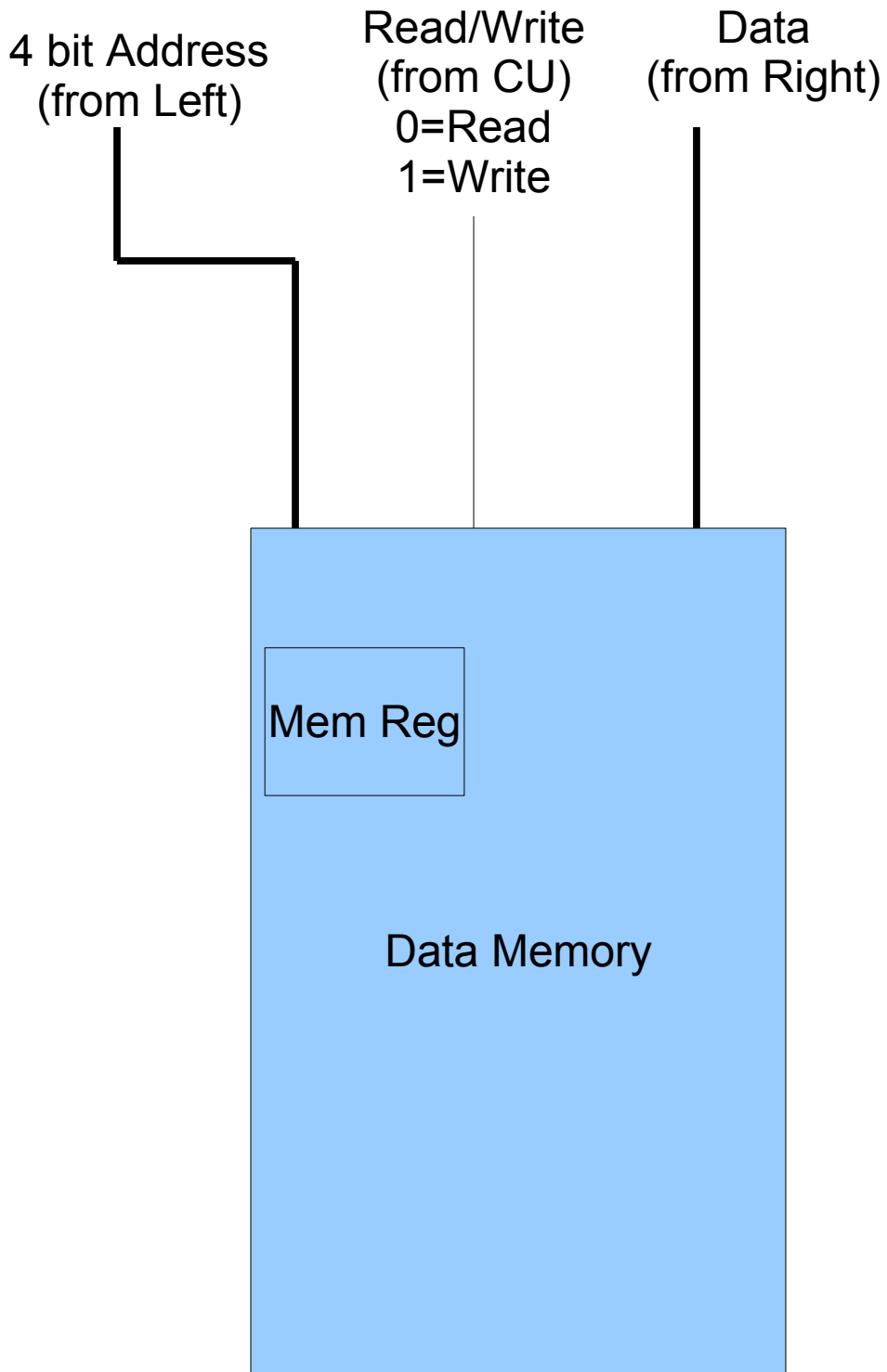
Sign Shrink

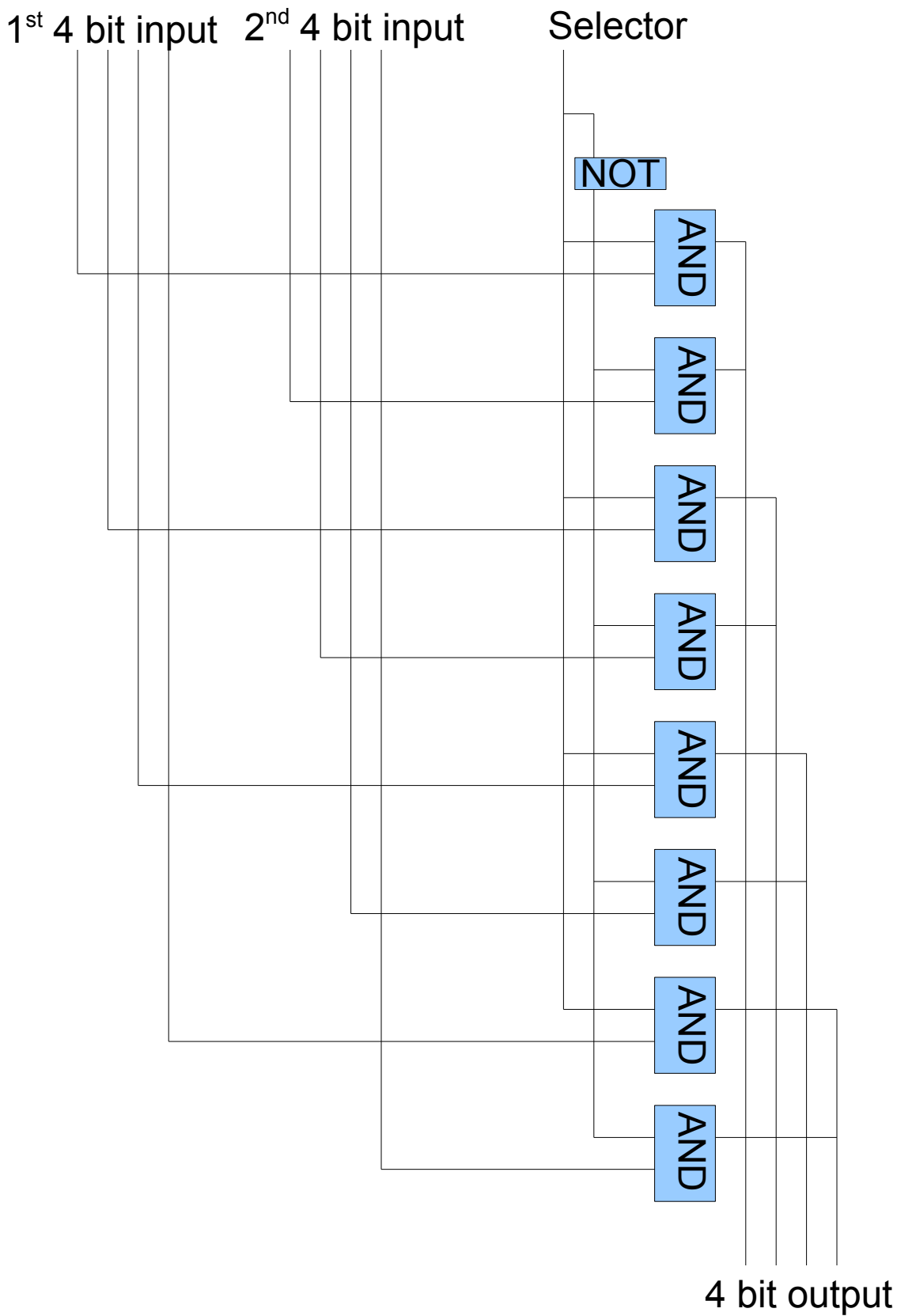


Sign Shrink Box (4 bit input, 2 bit output)



# Memory Black Box

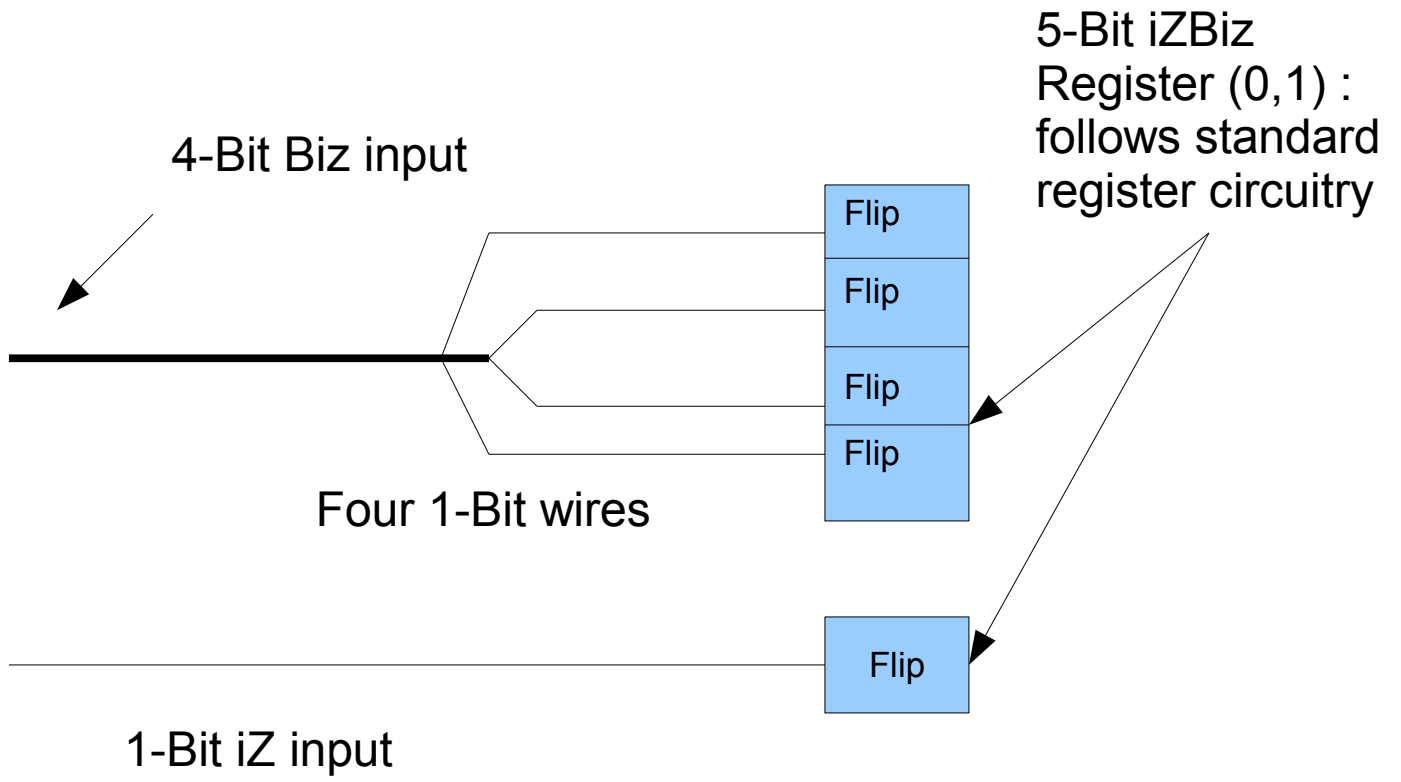




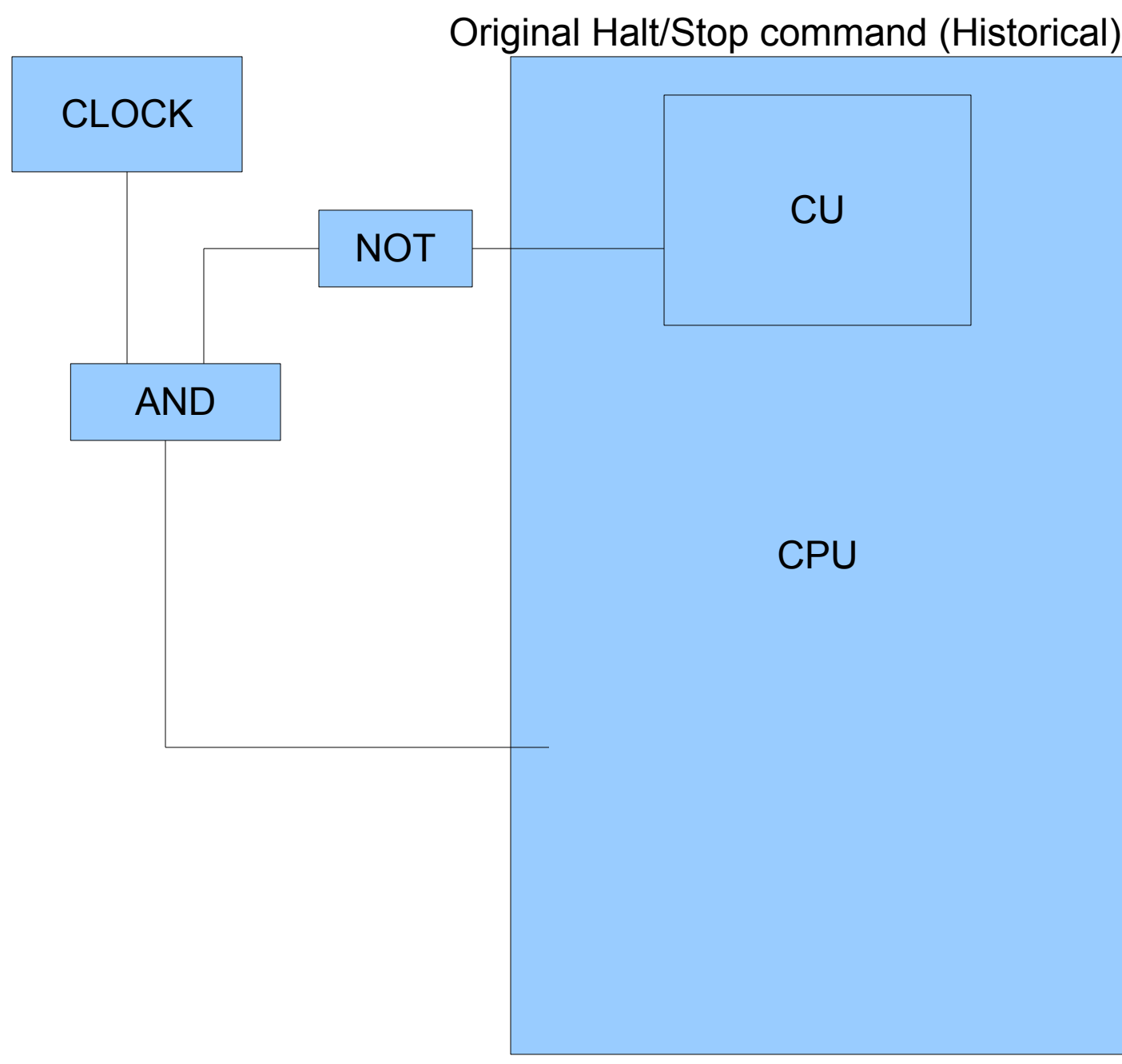
Mux Black Box (2 4 bit and 1 selector bit inputs, 4 outputs)



# Intermediate view of the iZBiz Register (0, 1)



# APPENDIX C : First attempt at HALT and STOP



# APPENDIX D: FIRST ATTEMPT AT ALU

